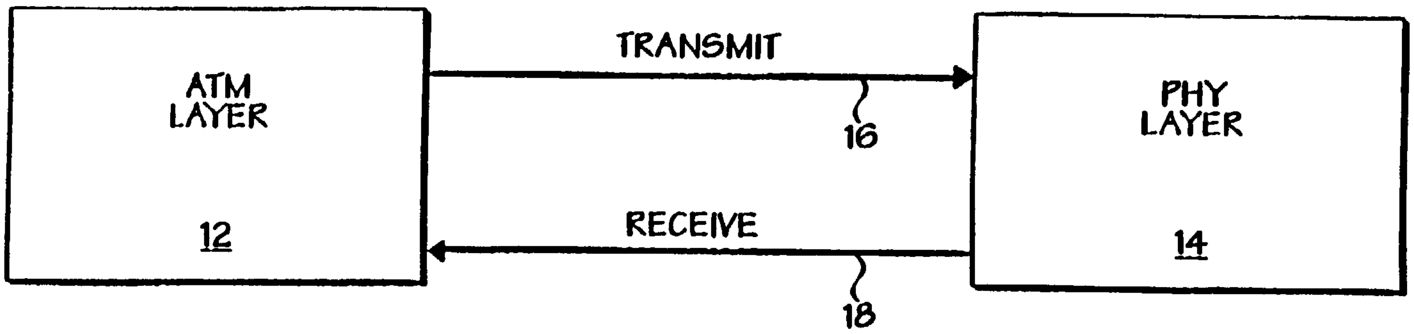


Fig. 1a
(PRIOR ART)

SCANNED, # 6

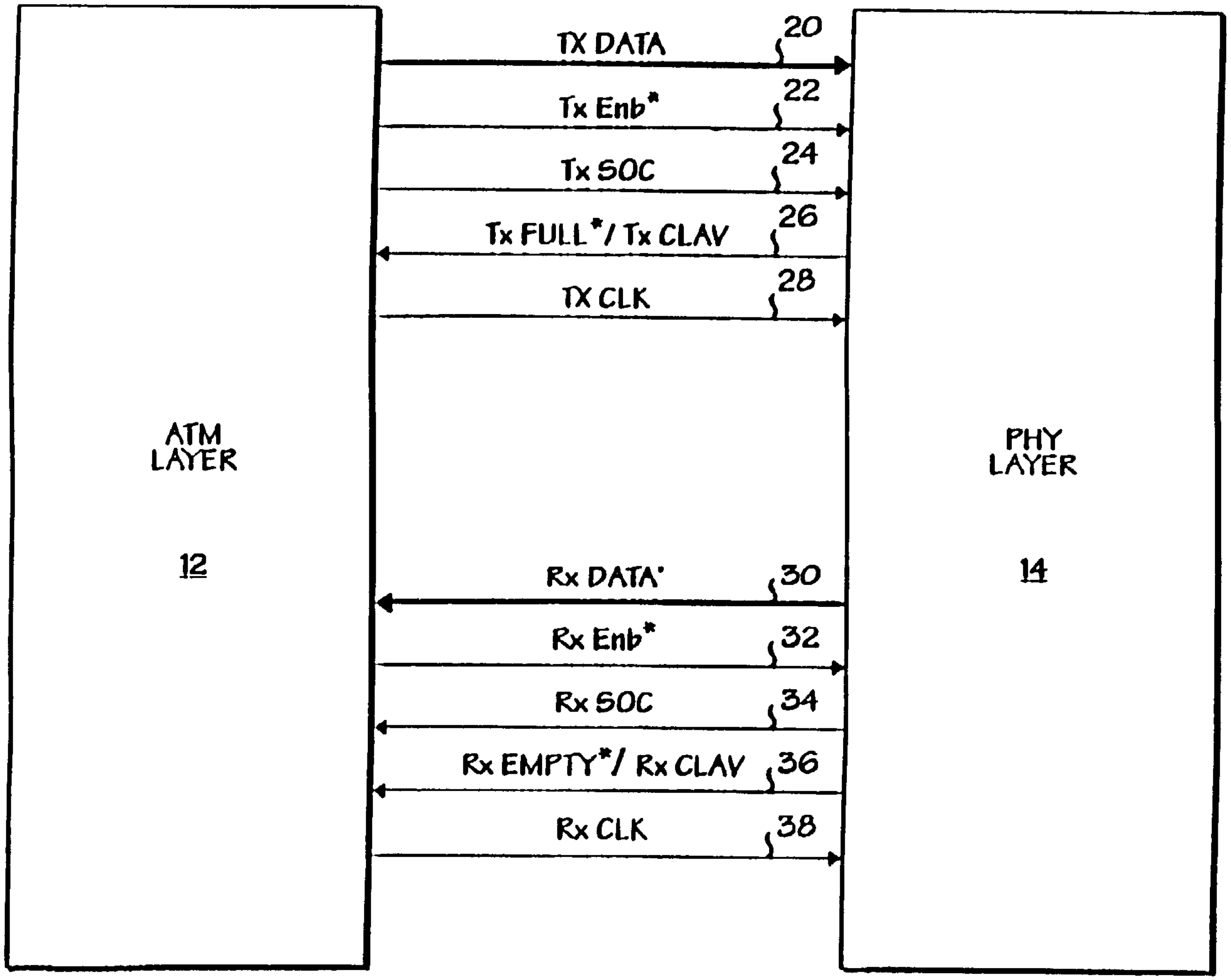


Fig. 1b
(PRIOR ART)

FIGURE 2a

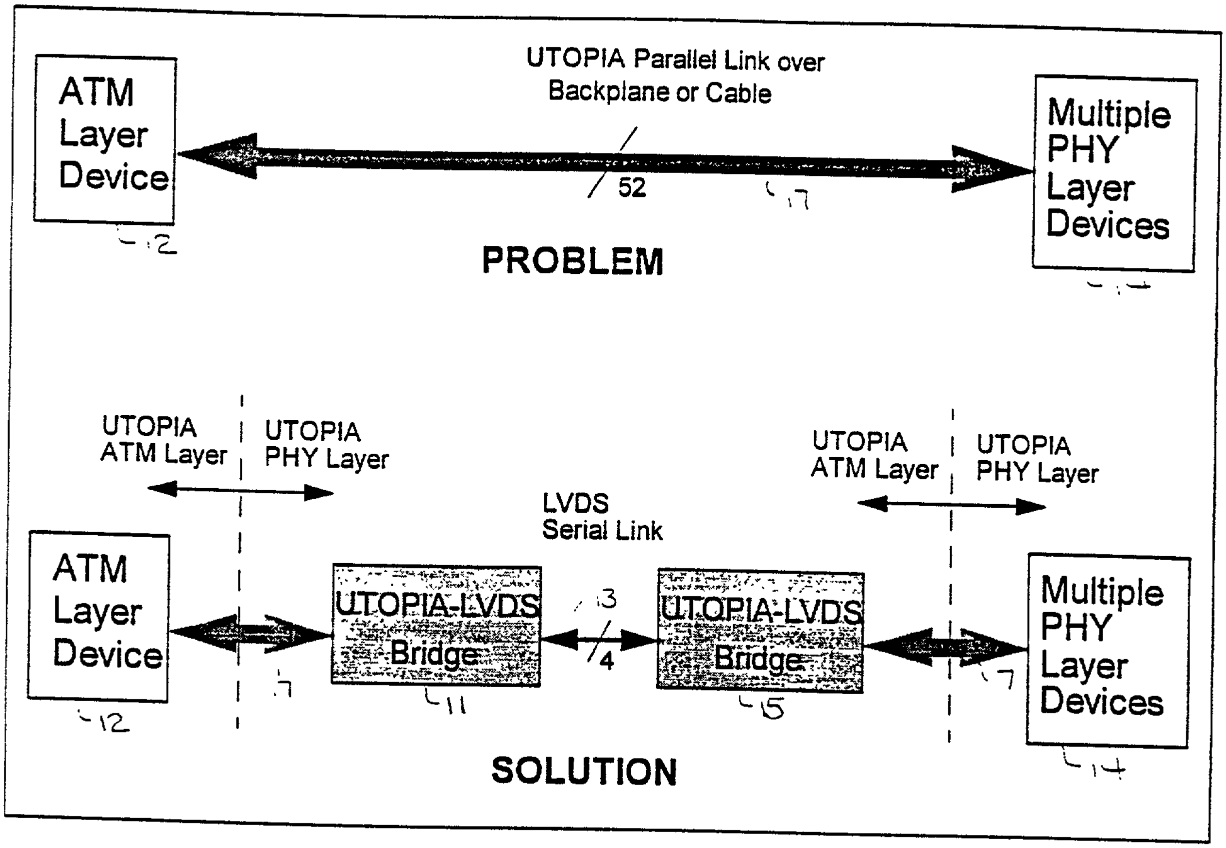
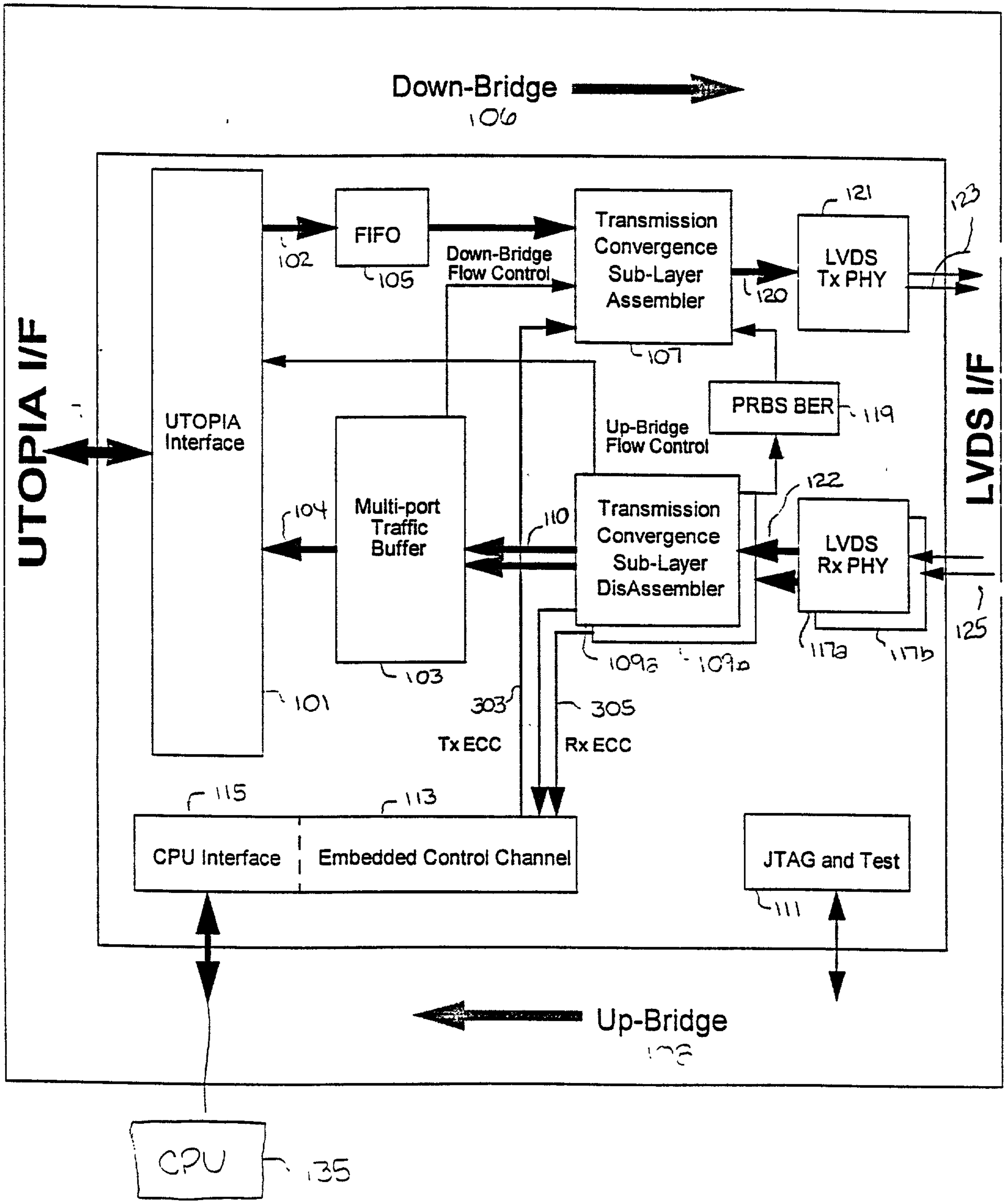


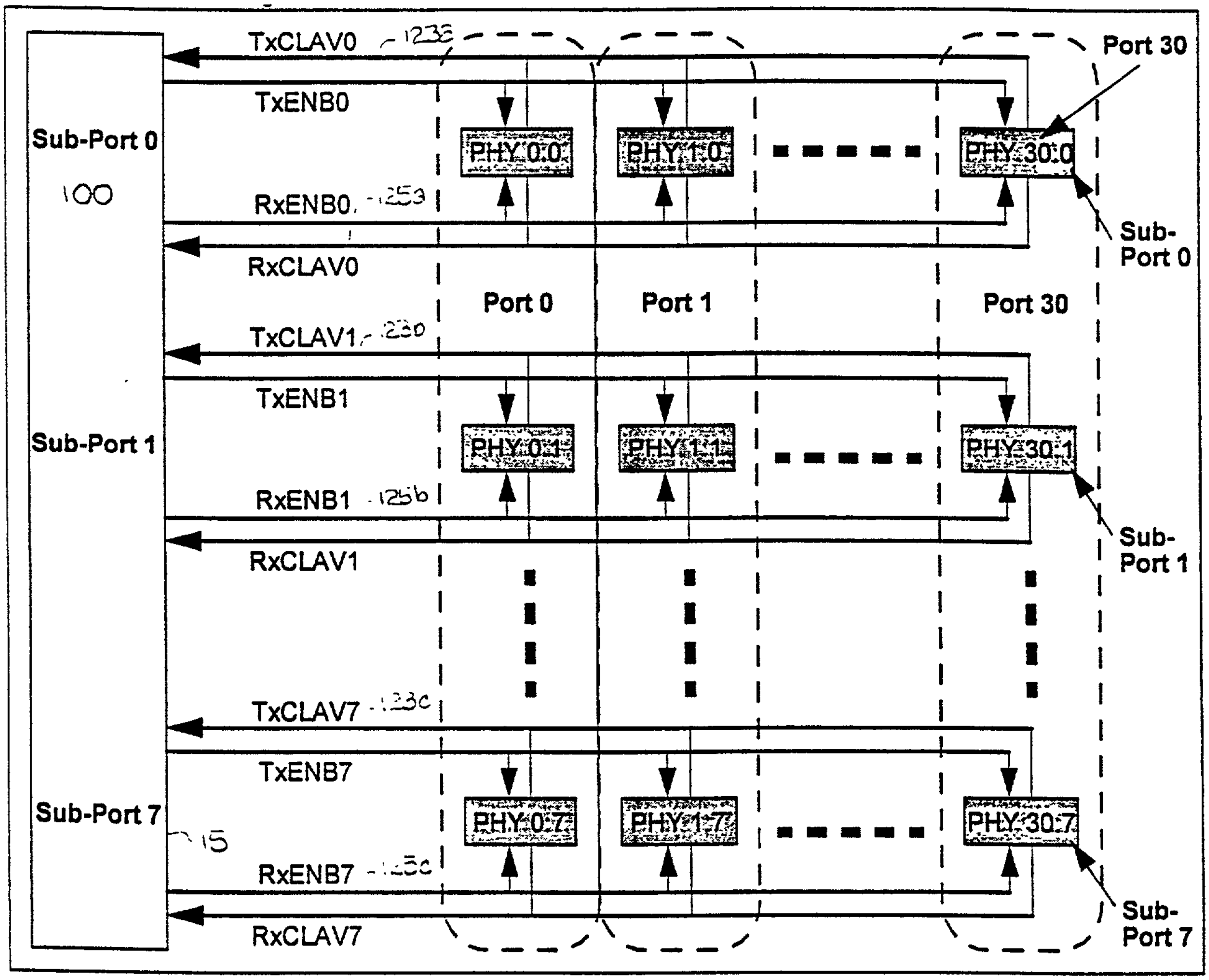
FIGURE 2b

FIGURE 3



Down-Bridge
106
UTOPIA I/F
UTOPIA Interface
101
102
FIFO
105
Down-Bridge Flow Control
Transmission Convergence Sub-Layer Assembler
107
120
LVDS Tx PHY
121
123
LVDS I/F
PRBS BER
119
Up-Bridge Flow Control
Multi-port Traffic Buffer
103
104
110
Transmission Convergence Sub-Layer DisAssembler
122
LVDS Rx PHY
125
117a
117b
109a
109b
303
305
Tx ECC
Rx ECC
115
113
CPU Interface
Embedded Control Channel
JTAG and Test
111
Up-Bridge
108
CPU
135

FIGURE 4



TxCLAV0
1238
TxENB0
Sub-Port 0
100
RxENB0
1253
RxCLAV0
PHY 0:0
PHY 1:0
PHY 30:0
Port 30
Sub-Port 0
Port 0
Port 1
Port 30
TxCLAV1
1230
TxENB1
Sub-Port 1
RxENB1
125b
RxCLAV1
PHY 0:1
PHY 1:1
PHY 30:1
Sub-Port 1
TxCLAV7
123c
TxENB7
Sub-Port 7
15
RxENB7
125c
RxCLAV7
PHY 0:7
PHY 1:7
PHY 30:7
Sub-Port 7

FIGURE 5

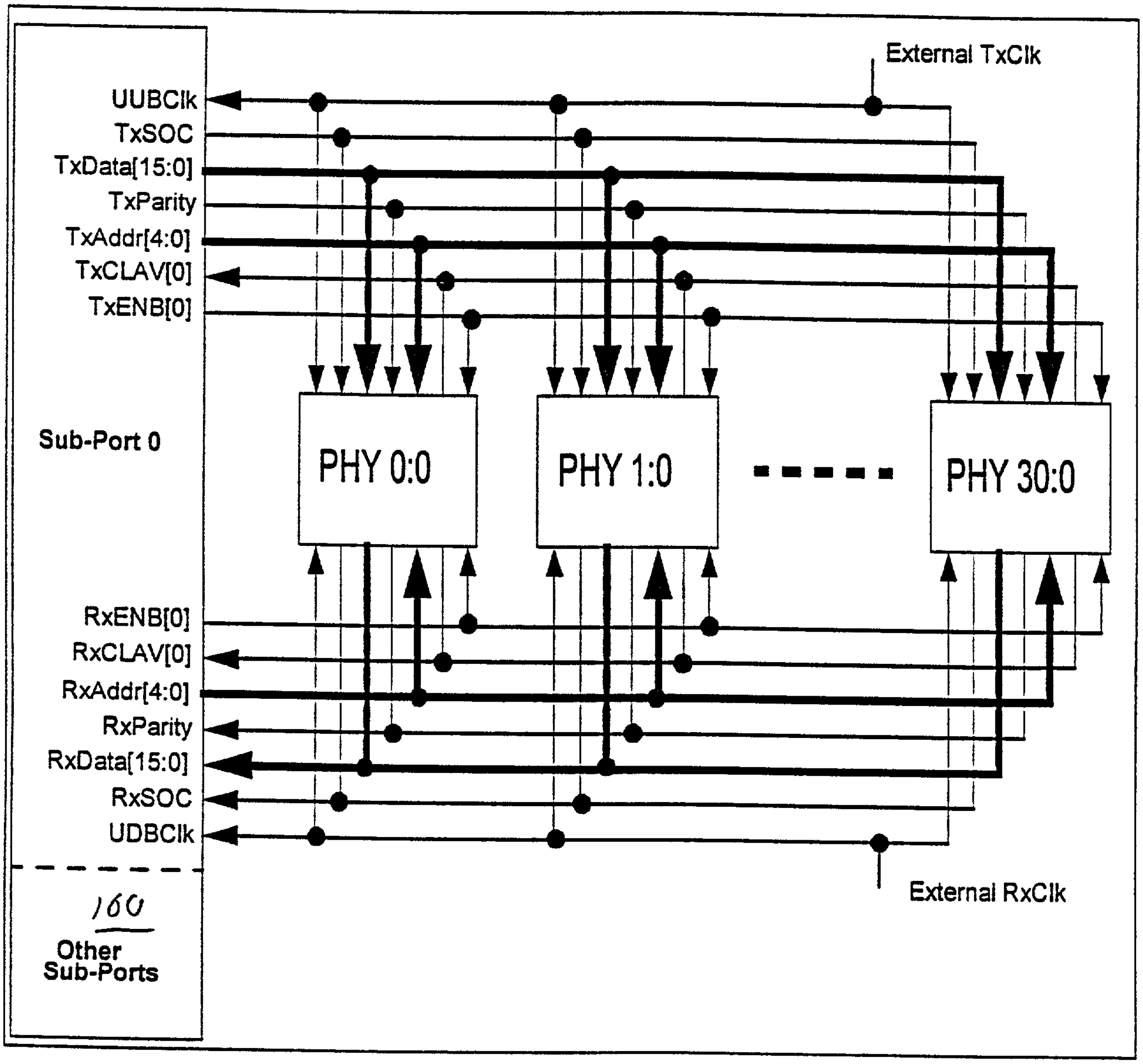
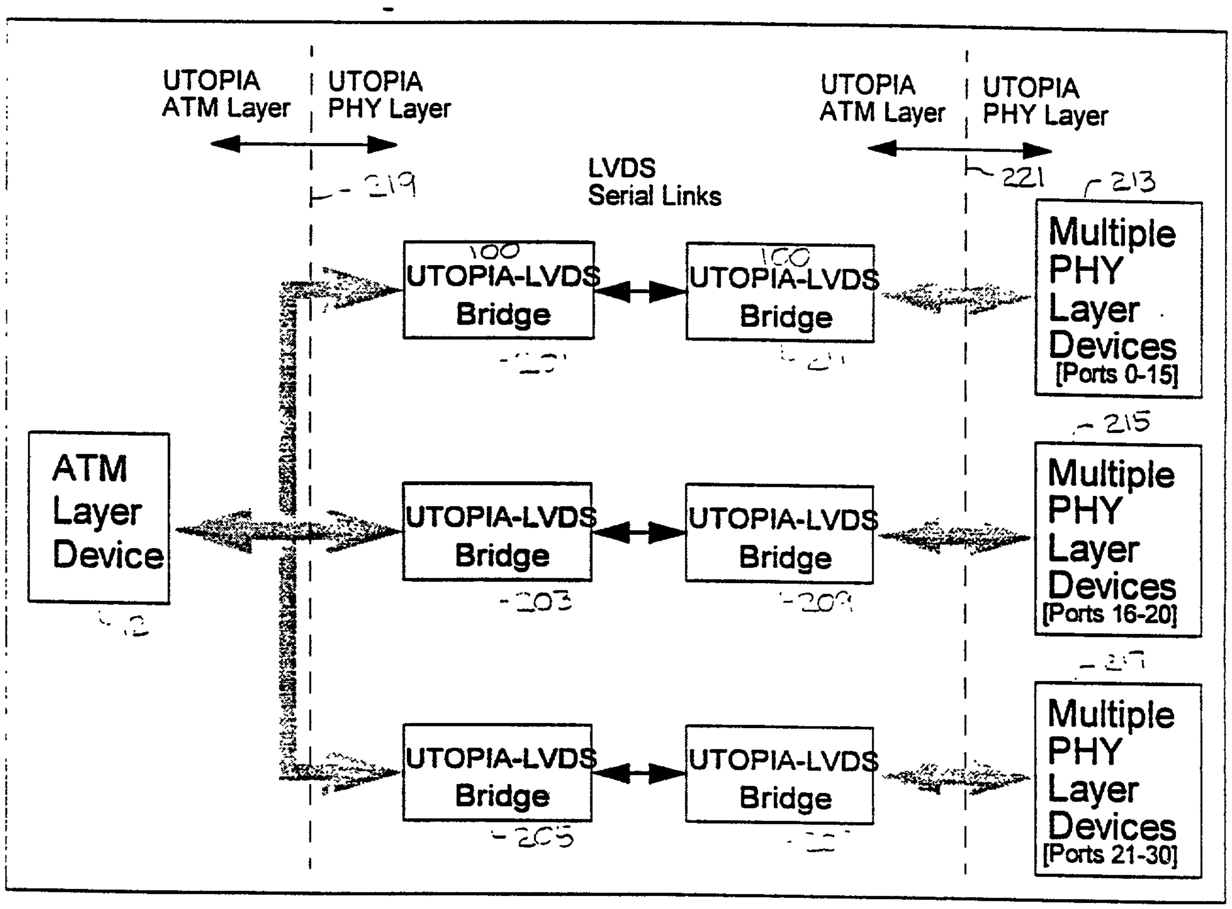

External TxClk
UUBClk
TxSOC
TxData[15:0]
TxParity
TxAddr[4:0]
TxCLAV[0]
TxENB[0]
Sub-Port 0
PHY 0:0
PHY 1:0
PHY 30:0
RxENB[0]
RxCLAV[0]
RxAddr[4:0]
RxParity
RxData[15:0]
RxSOC
UDBClk
External RxClk
160
Other Sub-Ports

FIGURE 6



UTOPIA ATM Layer
UTOPIA PHY Layer
219
UTOPIA ATM Layer
UTOPIA PHY Layer
221
LVDS Serial Links
213
ATM Layer Device
12
100
UTOPIA-LVDS Bridge
201
100
UTOPIA-LVDS Bridge
211
Multiple PHY Layer Devices [Ports 0-15]
215
UTOPIA-LVDS Bridge
203
UTOPIA-LVDS Bridge
209
Multiple PHY Layer Devices [Ports 16-20]
217
UTOPIA-LVDS Bridge
205
UTOPIA-LVDS Bridge
207
Multiple PHY Layer Devices [Ports 21-30]

FIGURE 7

Field	Fixed/Variable	Bytes
User Prepend	Variable	0, 2, 4, 6, 8, 10, 12
Cell Header	Fixed	4
UDF 1/2	Variable (On/Off)	2, 0 in 16 bit mode 1, 0 in 8 bit mode
Payload	Fixed	48
User Append	Variable	0, 2, 4, 6, 8, 10, 12

FIGURE 8

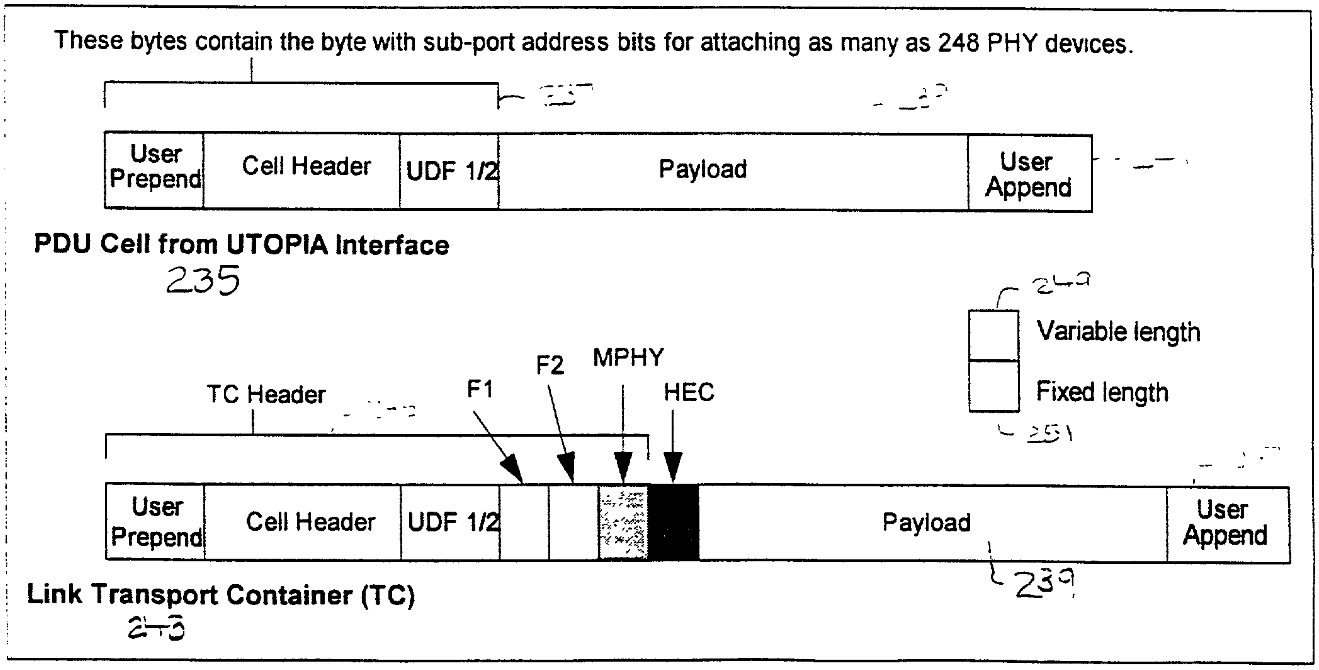


FIGURE 9

Bit	7	6	5	4	3	2	1	0
Function	MPHY Port Address 0-31					Reserved		

FIGURE 10

Flow Control 3		Flow Control 2	Flow Control 1	Flow Control 0
Res	Ports 30 - 24	Ports 23 - 16	Ports 15- 8	Ports 7 - 0

FIGURE 11

TC0 Flow Control 3 Flow Control 2	**TC1** Flow Control 1 Flow Control 0	**TC2** Flow Control 3 Flow Control 2	**TC3** Flow Control 1 Flow Control 0	**TC4** Flow Control 3 Flow Control 2	**TC5** Flow Control 1 Flow Control 0	**TC6** Alarm/Sig. Link Labels
TC7 Flow Control 3 Flow Control 2	**TC8** Flow Control 1 Flow Control 0	**TC9** Flow Control 3 Flow Control 2	**TC10** Flow Control 1 Flow Control 0	**TC11** Flow Control 3 Flow Control 2	**TC12** Flow Control 1 Flow Control 0	**TC13** ECC1 ECC2
TC14 Flow Control 3 Flow Control 2	**TC15** Flow Control 1 Flow Control 0	**TC16** Flow Control 3 Flow Control 2	**TC17** Flow Control 1 Flow Control 0	**TC18** Flow Control 3 Flow Control 2	**TC19** Flow Control 1 Flow Control 0	**TC20** ECC3 ECC4
TC21 Flow Control 3 Flow Control 2	**TC22** Flow Control 1 Flow Control 0	**TC23** Flow Control 3 Flow Control 2	**TC24** Flow Control 1 Flow Control 0	**TC25** Flow Control 3 Flow Control 2	**TC26** Flow Control 1 Flow Control 0	**TC27** BIP16
TC28 Flow Control 3 Flow Control 2	**TC29** Flow Control 1 Flow Control 0	**TC30** Flow Control 3 Flow Control 2	**TC31** Flow Control 1 Flow Control 0	**TC32** Flow Control 3 Flow Control 2	**TC33** Flow Control 1 Flow Control 0	**TC34** Reserved
TC35 Flow Control 3 Flow Control 2	**TC36** Flow Control 1 Flow Control 0	**TC37** Flow Control 3 Flow Control 2	**TC38** Flow Control 1 Flow Control 0	**TC39** Flow Control 3 Flow Control 2	**TC40** Flow Control 1 Flow Control 0	**TC41** ECC5 ECC6
TC42 Flow Control 3 Flow Control 2	**TC43** Flow Control 1 Flow Control 0	**TC44** Flow Control 3 Flow Control 2	**TC45** Flow Control 1 Flow Control 0	**TC46** Flow Control 3 Flow Control 2	**TC47** Flow Control 1 Flow Control 0	**TC48** ECC7 ECC8
TC49 Flow Control 3 Flow Control 2	**TC50** Flow Control 1 Flow Control 0	**TC51** Flow Control 3 Flow Control 2	**TC52** Flow Control 1 Flow Control 0	**TC53** Flow Control 3 Flow Control 2	**TC54** Flow Control 1 Flow Control 0	**TC55** BIP16

FIGURE 12

Bit	7	6	5	4	3	2	1	0
Function	RLOSA	RLOSB	RBA	RDSLL	EVN	ESSA	ESSB	Res

FIGURE 13

Number of Transport Containers in Frame (8 rows x 7 columns)	56
Bytes per Frame for Remote Alarms and Signalling	1
Bytes per Frame for Link Label	1
Bytes per Frame for ECC	8
Bytes per Frame Reserved	2
Bytes per Frame for BIP16	4
Bytes per Frame for OAM	16
Bytes per Frame for Flow Control	96
Bytes per Frame for F Channel	112

FIGURE 14

Link BW - Mbps	800	800
Container size - Bytes	56	68
Remote alarm BW - Mbps	0.26	0.21
Link Label BW - Mbps	0.26	0.21
ECC BW - Mbps	2.04	1.68
Reserved BW - Mbps	0.51	0.42
BIP16 BW - Mbps	1.02	0.84
OAM BW - Mbps	4.08	3.36
Flow Control BW - Mbps	24.49	20.17
F Channel BW - Mbps	28.57	23.53

FIGURE 15

Link BW - Mbps	800	800
Container size - Bytes	56	68
Remote alarm BW%	0.03	0.03
Link Label BW%	0.03	0.03
ECC BW%	0.26	0.21
Reserved BW%	0.06	0.05
BIP16 BW%	0.13	0.10
OAM BW%	0.51	0.42
Flow Control BW%	3.06	2.52
F Channel BW%	3.57	2.94

FIGURE 16

Meaning	Sequence	Address	Data
UNLOCK Sequence	1st write	0x00	0x00
	2nd write	0x01	0xFF
LOCK Sequence	1st write	0x00	0xDE
	2nd write	0x01	0xAD

FIGURE 17

Performance Counter	Associated Alarm	Comments
RAHECC2 - RAHECC0 (Section 7.27)	RAXHEC - Rx Port A Excessive HEC Errors. (Section 7.31)	Rx Port A 24-bit errored HEC counter. Mission mode Up-Bridge receive direction HEC monitoring.
RABIPC2 - RABIPC0 (Section 7.29)	RAXBIP - Rx Port A Excessive BIP Errors. (Section 7.31)	Rx Port A 24-bit errored BIP counter. Mission mode link error monitoring.
RABEC2 - RABEC0 (Section 7.39)	None.	Rx Port A 24-bit Bit Error Counter. Non-mission mode Bit Error counter with PRBS data over LVDS link.
RBHECC2 - RBHECC0 (Section 7.46)	RBXHEC - Rx Port B Excessive HEC Errors. (Section 7.50)	Rx Port B 24-bit errored HEC counter. Mission mode Up-Bridge receive direction HEC monitoring.
RBBIPC2 - RBBIPC0 (Section 7.48)	RBXBIP - Rx Port B Excessive BIP Errors. (Section 7.50)	Rx Port B 24-bit errored BIP counter. Mission mode link error monitoring.
RBBEC2 - RBBEC0 (Section 7.58)	None.	Rx Port b 24-bit Bit Error Counter. Non-mission mode Bit Error counter with PRBS data over LVDS link.
RAU2DLBC (Section 7.35)	U2DLBC - Up-2-Down Loopback Cell Count Change. Loopback cell(s) received on LVDS interface. (Section 7.72)	Rx Port A 8-bit Loopback cell counter. Mission mode diagnostic aid.
RBU2DLBC (Section 7.54)	U2DLBC - Up-2-Down Loopback Cell Count Change. Loopback cell(s) received on LVDS interface. (Section 7.72)	Rx Port B 8-bit Loopback cell counter. Mission mode diagnostic aid.
D2ULBCC (Section 7.71)	D2ULBC - Down-2-Up Loopback Cell Count Change. Loopback cell(s) received on UTOPIA interface. (Section 7.72)	UTOPIA Interface 8-bit Loopback cell counter. Mission mode diagnostic aid.

FIGURE 18A

Alarms	Description
LLOSC (Section 7.10)	Change of Status on LLOSA or LLOSB.
LLOSA (Section 7.10)	Loss of Signal on LVDS receive Port A.
LLOSB (Section 7.10)	Loss of Signal on LVDS receive Port B.
ETXBR (Section 7.10)	ECC transmit buffer ready for new message.
RALLC (Section 7.23)	Receive Port A. Link Label Change of value.
RALLM (Section 7.23)	Receive Port A. Link Label Mismatch between expected and received value.
RALCS (Section 7.23)	Receive Port A. Change of Status on RALDSLL, RALTCLL or RALFLL.
RALDSLL (Section 7.23)	Receive Port A. Descrambler Loss of Lock.
RALTCLL (Section 7.23)	Receive Port A. Transport Container delineation Loss of Lock.
RALFLL (Section 7.23)	Receive Port A. Frame delineation Loss of Lock.
ERABF (Section 7.23)	Receive Port A. ECC Receive Buffer Full - contains valid new message.
RARCS (Section 7.33)	Receive Port A. Remote Change of Status on RARLOSA, RARLOSB, RARBA or RARDSLL.
RARLOSA (Section 7.33)	Receive Port A. Remote Loss of Signal on LVDS receive Port A.
RARLOSB (Section 7.33)	Receive Port A. Remote Loss of Signal on LVDS receive Port B.
RARBA (Section 7.33)	Receive Port A. Remote Active receive port B or A.
RARDSLL (Section 7.33)	Receive Port A. Remote Descrambler Loss of Lock.
RBLLC (Section 7.42)	Receive Port B. Link Label Change of value.
RBLLM (Section 7.42)	Receive Port B. Link Label Mismatch between expected and received value.
RBLCS (Section 7.42)	Receive Port B. Change of Status on RBLDSLL, RBLTCLL or RBLFLL.
RBLDSLL (Section 7.42)	Receive Port B. Descrambler Loss of Lock.
RBLTCLL (Section 7.42)	Receive Port B. Transport Container delineation Loss of Lock.
RBLFLL (Section 7.42)	Receive Port B. Frame delineation Loss of Lock.
ERBBF (Section 7.42)	Receive Port B. ECC Receive Buffer Full - contains valid new message.
RBRCS (Section 7.52)	Receive Port B. Remote Change of Status on RBRLOSA, RBRLOSB, RBRBA or RBRDSLL.

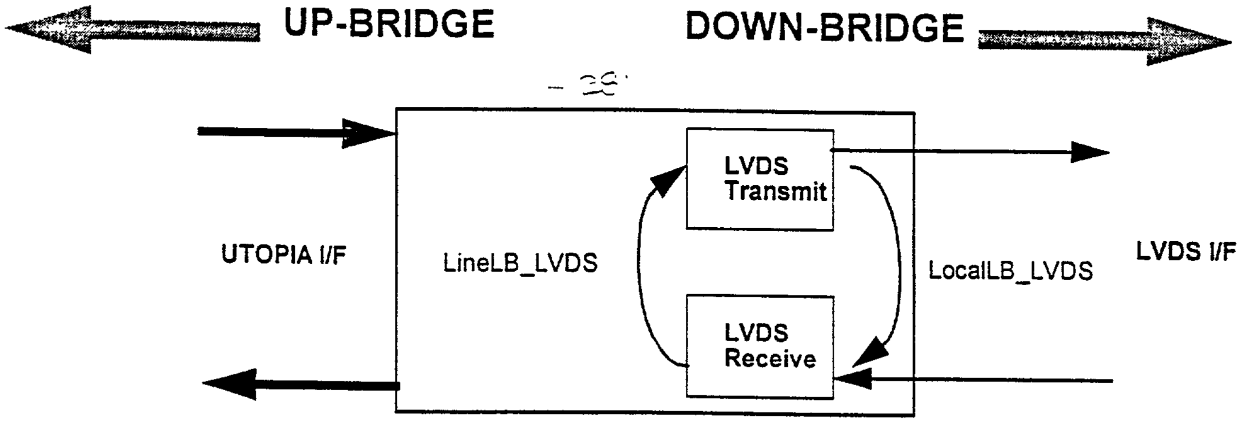
FIGURE 18β

RBRLOSA (Section 7.52)	Receive Port B. Remote Loss of Signal on LVDS receive Port A.
RBRLOSB (Section 7.52)	Receive Port B. Remote Loss of Signal on LVDS receive Port B.
RBRBA (Section 7.52)	Receive Port B. Remote Active receive port B or A.
RBRDSLL (Section 7.52)	Receive Port B. Remote Descrambler Loss of Lock.
PDULA (Section 7.72)	PDU Length greater than 64 bytes.
CTFRA (Section 7.72)	Cell Transfer error on UTOPIA interface.
UPRTY (Section 7.72)	Parity error detected on UTOPIA interface.
FIBOVA (Section 7.72)	FIB buffer overflow (down-bridge).
MTBSOVA (Section 7.72)	MTB Soft Overflow. One or more of the 31 MTB queues has exceeded its programmed threshold (up-bridge).
MTBHOVA (Section 7.72)	MTB Hard Overflow. The MTB queue has overflowed (up-bridge).

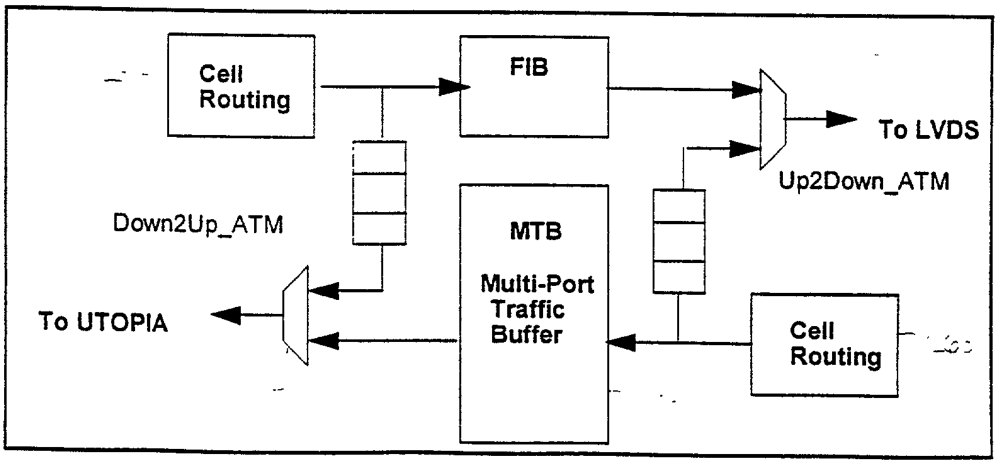
FIGURE 19

LineLB_LVDS	Physical loopback at the LVDS interface. Loop traffic entering the LVDS interface back out of the device.
LocalLB_LVDS	Physical loopback at the LVDS interface. Loop traffic exiting the LVDS interface back into the device.
Up2Down_ATM	ATM loopback. Route defined cell entering the device at the LVDS interface back out.
Down2Up_ATM	ATM loopback. Route defined cell entering the device at the UTOPIA interface back out.

FIGURE 20



(a) Physical Interface Loopbacks



(b) ATM Loopbacks

FIGURE 21 A

Signal Name	Description	Width	Signal Type	Polarity	Notes
UTOPIA INTERFACE					
U_TxData [15:0]	Transmit data bus.	16	BiDir [note 2]		
U_TxParity	Transmit data bus parity bit.	1	BiDir [note 2]		
U_TxCLAV [7:1]	Transmit cell available - Extended.	7	Input [note 3]	Active High	Pull Down
U_TxCLAV [0]	Transmit cell available - Normal/Extended.	1	BiDir [note 1]	Active High	Pull Down
U_TxENB [7:1]	Enable Data transfers - Extended.	7	Output [note 3]	Active Low	
U_TxENB [0]	Enable Data transfers - Normal/Extended.	1	BiDir [note 2]	Active Low	
U_TxSOC	Transmit Start Of Cell.	1	BiDir [note 2]	Active High	
U_TxAddr[4:0]	Address of MPHY device being selected.	5	BiDir [note 2]		
U_RxData [15:0]	Receive data bus.	16	BiDir [note 1]		
U_RxParity	Receive data bus parity bit.	1	BiDir [note 1]		
U_RxCLAV [7:1]	Receive cell available - Extended.	7	Input [note 3]	Active High	Pull Down
U_RxCLAV [0]	Receive cell available - Normal/Extended.	1	BiDir [note 1]	Active High	Pull Down
U_RxENB [7:1]	Enable Data transfers - Extended.	7	Output [note 3]	Active Low	
U_RxENB [0]	Enable Data transfers - Normal/Extended.	1	BiDir [note 2]	Active Low	
U_RxSOC	Receive Start Of Cell.	1	BiDir [note 1]	Active High	
U_RxAddr[4:0]	Address of MPHY device being selected.	5	BiDir [note 2]		
U_UDBClk	Input transfer clock.	1	Input[note 4]		
U_UUBClk	Output transfer clock.	1	Input[note 5]		
LVDS INTERFACE					
LVDS_ADout[+,-]	A Serial data differential outputs.	2	Output		
LVDS_BDout[+,-]	B Serial data differential outputs.	2	Output		
LVDS_ADenb	Serial transmit data A output enable.	1	Input	Active High	Pull Up
LVDS_BDenb	Serial transmit data B output enable.	1	Input	Active High	Pull Up
LVDS_TxPwdn	Transmit section Power Down.	1	Input	Active Low	Pull Up
LVDS_Synch	External control for transmission of SYNCH patterns on serial interface.	1	Input	Active High	Pull Down
LVDS_TxClk	Transmit clock.	1	Input		
LVDS_ADin[+,-]	Port A Serial data differential inputs.	2	Input		
LVDS_ALock_n	PortA Clock recovery lock status.	1	Output		
LVDS_ARxClk	PortA Recovered clock.	1	Output		
LVDS_ARefClk	PortA Reference clock for receive PLLs.	1	Input		
LVDS_APwdn	PortA Power Down.	1	Input	Active Low	Pull Up

FIGURE 21B

LVDS_BDin[+,-]	PortB Serial data differential inputs.	2	Input		
LVDS_BLock_n	PortB Clock recovery lock status.	1	Output		
LVDS_BRxClk	PortB Recovered clock.	1	Output		
LVDS_BRefClk	PortB Reference clock for receive PLLs.	1	Input		
LVDS_BPwdn	PortB Power Down.	1	Input	Active Low	Pull Up
Reserved	Reserved for divide by 2 of recovered clock.	1	Output		
Reserved	Reserved for 8kHz from recovered clock.	1	Output		
CPU & GENERAL CONTROL					
CPU_cs	Select signal used to validate the address bus for read and write data transfers.	1	Input	Active Low	
CPU_rd (CPU_ds)	Read or Data Strobe, depending on CPU_BusMode.	1	Input	Active Low	
CPU_wr (CPU_rnw)	Write or Read/Write, depending on CPU_BusMode.	1	Input	Active Low (Write)	
CPU_int	Interrupt request line.	1	Output	Active Low	Open Drain
CPU_Data[7:0]	Data bus.	8	BiDir		
CPU_Addr[7:0]	Address bus.	8	Input		
CPU_BusMode	Mode select for bus protocol.	1	Input		Pull Down
GPIO [3:0]	General Purpose Input/Output.	4	BiDir		
Reset_n	Chip reset.	1	Input	Active Low	Pull Up
JTAG TEST INTERFACE					
JTAG_CLK	Test clock.	1	Input		
JTAG_Reset	Test circuit reset.	1	Input	Active Low	Pull Up
JTAG_TMS	Test Mode Select.	1	Input		Pull Up
JTAG_TDI	Test Data In.	1	Input		
JTAG_TDO	Test Data Out.	1	Output		
Test_se	Scan enable.	1	Input	Active High	Pull Down
Test_bus	Internal Data Bus access between UTOPIA and LVDS sections	16	BiDir note 6 note 7		
Test_bus_dir	Test Data Bus Direction	1	Input note 7		Pull Up
Test_bus_sel	Test Data bus output mux select	3	Input note 7		Pull Down
Functional I/O		**135**			
LVDS VDD/VSS	**3.3v LVDS power**	**43**			
LS VDD	**3.3v Level Shifter power**	**2**			
ESD		**1**			
CVDD/CVSS	**2.5v Core Power**	**6**			

FIGURE 21

IOVDD/IOVSS	3.3v I/O ring power	8
Total Power		61
Spare		1
TOTAL PINS		196

FIGURE 22 A

Register Name	Address	Software Lock	Reset Value	Section and Description
SLK0	0x00	N	0x00	7.1 Software Lock 1
SLK1	0x01	N	0x00	7.1 Software Lock 2
VID	0x02	N	0x01	7.2 Version Identification
GCS	0x03	Y	0x05	7.3 General Control and Status
LVC	0x04	Y	0x3B	7.4 LVDS Control
PDUCFG	0x05	Y	0x00	7.5 PDU Configuration
IS	0x06	N	0x00	7.6 Interrupt Source
ISE	0x07	N	0x00	7.7 Interrupt Source Enables
LKSC	0x08	Y	0x3B	7.8 Link Status and Control
TXLL	0x09	N	0x00	7.9 Transmit Link Label
ETXRXA	0x0A	N	0x01	7.10 ECC Transmit Buffer and Receive LVDS Alarms
ETXRXIE	0x0B	N	0x00	7.11 ECC Transmit Buffer and Receive LVDS Interrupt Enables
ETXSD	0x0C	N	0x00	7.12 ECC Transmit Buffer Send
ETXD7	0x0D	N	0x00	7.13 ECC Transmit Buffer 7
ETXD6	0x0E	N	0x00	7.13 ECC Transmit Buffer 6
ETXD5	0x0F	N	0x00	7.13 ECC Transmit Buffer 5
ETXD4	0x10	N	0x00	7.13 ECC Transmit Buffer 4
ETXD3	0x11	N	0x00	7.13 ECC Transmit Buffer 3
ETXD2	0x12	N	0x00	7.13 ECC Transmit Buffer 2
ETXD1	0x13	N	0x00	7.13 ECC Transmit Buffer 1
ETXD0	0x14	N	0x00	7.13 ECC Transmit Buffer 0
GPIO	0x15	N	0xF0	7.14 General Purpose Input/Output
TERRCTL	0x16	Y	0x00	7.15 Test Error Control
ERRBIP1	0x17	Y	0x00	7.16 BIP Error Mask 1
ERRBIP0	0x18	Y	0x00	7.16 BIP Error Mask 0
ERRHEC	0x19	Y	0x00	7.17 HEC Error Mask 0
ALBC	0x1A	N	0x00	7.18 ATM and LVDS Loopback Control
ALBMP	0x1B	N	0x00	7.19 ATM Loopback Cell MPhy
ALBCF3	0x1C	N	0x00	7.20 ATM Loopback Cell Format 3
ALBCF2	0x1D	N	0x00	7.20 ATM Loopback Cell Format 2

FIGURE 22b

Register Name	Address	Software Lock	Reset Value	Section and Description
ALBCF1	0x1E	N	0x00	7.20 ATM Loopback Cell Format 1
ALBCF0	0x1F	N	0x00	7.20 ATM Loopback Cell Format 0
RALL	0x20	N	0x00	7.21 Receive Port A Link Label
RAELL	0x21	N	0x00	7.22 Receive Port A Expected Link Label
RALA	0x22	N	0x00	7.23 Receive Port A Local Alarms
RALIE	0x23	N	0x00	7.24 Receive Port A Local Interrupt Enables
RACTL	0x24	Y	0x01	7.25 Receive Port A Control
Reserved	0x25			
ERAD7	0x26	N	0x00	7.26 ECC Receive Buffer A 7
ERAD6	0x27	N	0x00	7.26 ECC Receive Buffer A 6
ERAD5	0x28	N	0x00	7.26 ECC Receive Buffer A 5
ERAD4	0x29	N	0x00	7.26 ECC Receive Buffer A 4
ERAD3	0x2A	N	0x00	7.26 ECC Receive Buffer A 3
ERAD2	0x2B	N	0x00	7.26 ECC Receive Buffer A 2
ERAD1	0x2C	N	0x00	7.26 ECC Receive Buffer A 1
ERAD0	0x2D	N	0x00	7.26 ECC Receive Buffer A 0
RAHECC2	0x2E	N	0x00	7.27 Receive Port A HEC Count 2
RAHECC1	0x2F	N	0x00	7.27 Receive Port A HEC Count 1
RAHECC0	0x30	N	0x00	7.27 Receive Port A HEC Count 0
RAHECT2	0x31	N	0xFF	7.28 Receive Port A HEC Threshold 2
RAHECT1	0x32	N	0xFF	7.28 Receive Port A HEC Threshold 1
RAHECT0	0x33	N	0xFF	7.28 Receive Port A HEC Threshold 0
RABIPC2	0x34	N	0x00	7.29 Receive Port A BIP Count 2
RABIPC1	0x35	N	0x00	7.29 Receive Port A BIP Count 1
RABIPC0	0x36	N	0x00	7.29 Receive Port A BIP Count 0
RABIPT2	0x37	N	0xFF	7.30 Receive Port A BIP Threshold 2
RABIPT1	0x38	N	0xFF	7.30 Receive Port A BIP Threshold 1
RABIPT0	0x39	N	0xFF	7.30 Receive Port A BIP Threshold 0
RAPA	0x3A	N	0x00	7.31 Receive Port A Performance Alarms
RAPIE	0x3B	N	0x00	7.32 Receive Port A Performance Interrupt Enables
RARA	0x3C	N	0x0D	7.33 Receive Port A Remote Alarms
RARIE	0x3D	N	0x00	7.34 Receive Port A Remote Interrupt Enables
RAU2DLBC	0x3E	N	0x00	7.35 Receive Port A ATM Up2Down Loopback Cell Count

FIGURE 22C

Register Name	Address	Software Lock	Reset Value	Section and Description
Unused	0x3F			
RACDT	0x40	Y	0x78	7.36 Receive Port A Cell Delineation Thresholds
RAFDT	0x41	Y	0x78	7.37 Receive Port A Frame Delineation Thresholds
RADSLKT	0x42	Y	0x88	7.38 Receive Port A Descrambler Lock Thresholds
RABEC2	0x43	N	0x00	7.39 Receive Port A Bit Error Count 2
RABEC1	0x44	N	0x00	7.39 Receive Port A Bit Error Count 1
RABEC0	0x45	N	0x00	7.39 Receive Port A Bit Error Count 0
Unused	0x46			
Reserved	0x47			
Reserved	0x48			
Unused	0x49 to 0x56			
Reserved	0x57			
Reserved	0x58			
Reserved	0x59			
Reserved	0x5A			
Unused	0x5B			
Reserved	0x5C			
Reserved	0x5D			
Reserved	0x5E			
Reserved	0x5F			
RBLL	0x60	N	0x00	7.40 Receive Port B Link Label
RBELL	0x61	N	0x00	7.41 Receive Port B Expected Link Label
RBLA	0x62	N	0x00	7.42 Receive Port B Local Alarms
RBLIE	0x63	N	0x00	7.43 Receive Port B Local Interrupt Enables
RBCTL	0x64	Y	0x01	7.44 Receive Port B Control
Reserved	0x65			
ERBD7	0x66	N	0x00	7.45 ECC Receive Buffer B 7
ERBD6	0x67	N	0x00	7.45 ECC Receive Buffer B 6
ERBD5	0x68	N	0x00	7.45 ECC Receive Buffer B 5
ERBD4	0x69	N	0x00	7.45 ECC Receive Buffer B 4
ERBD3	0x6A	N	0x00	7.45 ECC Receive Buffer B 3
ERBD2	0x6B	N	0x00	7.45 ECC Receive Buffer B 2

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FIGURE 22D

Register Name	Address	Software Lock	Reset Value	Section and Description
ERBD1	0x6C	N	0x00	7.45 ECC Receive Buffer B 1
ERBD0	0x6D	N	0x00	7.45 ECC Receive Buffer B 0
RBHECC2	0x6E	N	0x00	7.46 Receive Port B HEC Count 2
RBHECC1	0x6F	N	0x00	7.46 Receive Port B HEC Count 1
RBHECC0	0x70	N	0x00	7.46 Receive Port B HEC Count 0
RBHECT2	0x71	N	0xFF	7.47 Receive Port B HEC Threshold 2
RBHECT1	0x72	N	0xFF	7.47 Receive Port B HEC Threshold 1
RBHECT0	0x73	N	0xFF	7.47 Receive Port B HEC Threshold 0
RBBIPC2	0x74	N	0x00	7.48 Receive Port B BIP Count 2
RBBIPC1	0x75	N	0x00	7.48 Receive Port B BIP Count 1
RBBIPC0	0x76	N	0x00	7.48 Receive Port B BIP Count 0
RBBIPT2	0x77	N	0xFF	7.49 Receive Port B BIP Threshold 2
RBBIPT1	0x78	N	0xFF	7.49 Receive Port B BIP Threshold 1
RBBIPT0	0x79	N	0xFF	7.49 Receive Port B BIP Threshold 0
RBPA	0x7A	N	0x00	7.50 Receive Port B Performance Alarms
RBPIE	0x7B	N	0x00	7.51 Receive Port B Performance Interrupt Enables
RBRA	0x7C	N	0x0D	7.52 Receive Port B Remote Alarms
RBRIE	0x7D	N	0x00	7.53 Receive Port B Remote Interrupt Enables
RBU2DLBC	0x7E	N	0x00	7.54 Receive Port B ATM Up2Down Loopback Cell Count
Unused	0x7F			
RBCDT	0x80	Y	0x78	7.55 Receive Port B Cell Delineation Thresholds
RBFDT	0x81	Y	0x78	7.56 Receive Port B Frame Delineation Thresholds
RBDSLKT	0x82	Y	0x88	7.57 Receive Port B Descrambler Lock Thresholds
RBBEC2	0x83	N	0x00	7.58 Receive Port B Bit Error Count 2
RBBEC1	0x84	N	0x00	7.58 Receive Port B Bit Error Count 1
RBBEC0	0x85	N	0x00	7.58 Receive Port B Bit Error Count 0
Unused	0x86			
Reserved	0x87			
Reserved	0x88			
Unused	0x89 to 0x96			
Reserved	0x97			
Reserved	0x98			

FIGURE 22E

Register Name	Address	Software Lock	Reset Value	Section and Description
Reserved	0x99			
Reserved	0x9A			
Unused	0x9B			
Reserved	0x9C			
Reserved	0x9D			
Reserved	0x9E			
Reserved	0x9F			
UCFG	0xA0	Y	0x00	7.59 UTOPIA Configuration
UCPL3	0xA1	Y	0x7F	7.60 UTOPIA Connected Port List 3
UCPL2	0xA2	Y	0xFF	7.60 UTOPIA Connected Port List 2
UCPL1	0xA3	Y	0xFF	7.60 UTOPIA Connected Port List 1
UCPL0	0xA4	Y	0xFF	7.60 UTOPIA Connected Port List 0
Reserved	0xA5			
UCSPL	0xA6	Y	0x01	7.61 UTOPIA Connected Sub-Port List
USPAL	0xA7	Y	0x00	7.62 UTOPIA Sub-Port Address Location
USPAM	0xA8	Y	0x07	7.63 UTOPIA Sub-Port Address Mask
MTBQT30	0xA9	Y	0x04	7.64 MTB Queue Threshold 30
MTBQT29	0xAA	Y	0x04	7.64 MTB Queue Threshold 29
MTBQT28	0xAB	Y	0x04	7.64 MTB Queue Threshold 28
MTBQT27	0xAC	Y	0x04	7.64 MTB Queue Threshold 27
MTBQT26	0xAD	Y	0x04	7.64 MTB Queue Threshold 26
MTBQT25	0xAE	Y	0x04	7.64 MTB Queue Threshold 25
MTBQT24	0xAF	Y	0x04	7.64 MTB Queue Threshold 24
MTBQT23	0xB0	Y	0x04	7.64 MTB Queue Threshold 23
MTBQT22	0xB1	Y	0x04	7.64 MTB Queue Threshold 22
MTBQT21	0xB2	Y	0x04	7.64 MTB Queue Threshold 21
MTBQT20	0xB3	Y	0x04	7.64 MTB Queue Threshold 20
MTBQT19	0xB4	Y	0x04	7.64 MTB Queue Threshold 19
MTBQT18	0xB5	Y	0x04	7.64 MTB Queue Threshold 18
MTBQT17	0xB6	Y	0x04	7.64 MTB Queue Threshold 17
MTBQT16	0xB7	Y	0x04	7.64 MTB Queue Threshold 16
MTBQT15	0xB8	Y	0x04	7.64 MTB Queue Threshold 15
MTBQT14	0xB9	Y	0x04	7.64 MTB Queue Threshold 14

FIGURE 22F

Register Name	Address	Software Lock	Reset Value	Section and Description
MTBQT13	0xBA	Y	0x04	7.64 MTB Queue Threshold 13
MTBQT12	0xBB	Y	0x04	7.64 MTB Queue Threshold 12
MTBQT11	0xBC	Y	0x04	7.64 MTB Queue Threshold 11
MTBQT10	0xBD	Y	0x04	7.64 MTB Queue Threshold 10
MTBQT9	0xBE	Y	0x04	7.64 MTB Queue Threshold 9
MTBQT8	0xBF	Y	0x04	7.64 MTB Queue Threshold 8
MTBQT7	0xC0	Y	0x04	7.64 MTB Queue Threshold 7
MTBQT6	0xC1	Y	0x04	7.64 MTB Queue Threshold 6
MTBQT5	0xC2	Y	0x04	7.64 MTB Queue Threshold 5
MTBQT4	0xC3	Y	0x04	7.64 MTB Queue Threshold 4
MTBQT3	0xC4	Y	0x04	7.64 MTB Queue Threshold 3
MTBQT2	0xC5	Y	0x04	7.64 MTB Queue Threshold 2
MTBQT1	0xC6	Y	0x04	7.64 MTB Queue Threshold 1
MTBQT0	0xC7	Y	0x04	7.64 MTB Queue Threshold 0
MTBQFL3	0xC8	N	0x00	7.65 MTB Queue Full 3
MTBQFL2	0xC9	N	0x00	7.65 MTB Queue Full 2
MTBQFL1	0xCA	N	0x00	7.65 MTB Queue Full 1
MTBQFL0	0xCB	N	0x00	7.65 MTB Queue Full 0
MTBQE3	0xCC	N	0x7F	7.66 MTB Queue Empty 3
MTBQE2	0xCD	N	0xFF	7.66 MTB Queue Empty 2
MTBQE1	0xCE	N	0xFF	7.66 MTB Queue Empty 1
MTBQE0	0xCF	N	0xFF	7.66 MTB Queue Empty 0
MTBQF3	0xD0	Y	0x00	7.67 MTB Queue Flush 3
MTBQF2	0xD1	Y	0x00	7.67 MTB Queue Flush 2
MTBQF1	0xD2	Y	0x00	7.67 MTB Queue Flush 1
MTBQF0	0xD3	Y	0x00	7.67 MTB Queue Flush 0
MTBCF3	0xD4	Y	0x00	7.68 MTB Cell Flush 3
MTBCF2	0xD5	Y	0x00	7.68 MTB Cell Flush 2
MTBCF1	0xD6	Y	0x00	7.68 MTB Cell Flush 1
MTBCF0	0xD7	Y	0x00	7.68 MTB Cell Flush 0
QFL	0xD8	Y	0x00	7.69 Queue Flush
MTBQOV3	0xD9	N	0x00	7.70 MTB Queue Overflow 3
MTBQOV2	0xDA	N	0x00	7.70 MTB Queue Overflow 2

FIGURE 22G

Register Name	Address	Software Lock	Reset Value	Section and Description
MTBQOV1	0xDB	N	0x00	7.70 MTB Queue Overflow 1
MTBQOV0	0xDC	N	0x00	7.70 MTB Queue Overflow 0
Unused	0xDD to 0xDF			
D2ULBCC	0xE0	N	0x00	7.71 ATM Down2Up Loopback Cell Count
UAA	0xE1	N	0x00	7.72 UTOPIA and ATM Alarms
UAIE	0xE2	N	0x00	7.73 UTOPIA and ATM Interrupt Enables
Unused	0xE3 to 0xF6			
ALFLT3	0xF7	N	0xFF	7.74 ATM Loopback Cell Filter 3
ALFLT2	0xF8	N	0xFF	7.74 ATM Loopback Cell Filter 2
ALFLT1	0xF9	N	0xFF	7.74 ATM Loopback Cell Filter 1
ALFLT0	0xFA	N	0xFF	7.74 ATM Loopback Cell Filter 0
Unused	0xFB			
Reserved	0xFC			
Reserved	0xFD			
Reserved	0xFE			
Reserved	0xFF			

FIGURE 23

	7	6	5	4	3	2	1	0
SLK0 0X00	0	0	0	0	0	0	0	0
SLK1 0X01	0	0	0	0	0	0	0	0

FIGURE 24

7	6	5	4	3	2	1	0
VID[7]	VID[6]	VID[5]	VID[4]	VID[3]	VID[2]	VID[1]	VID[0]

FIGURE 25

7	6	5	4	3	2	1	0
Reserved	Reserved	GIE	LT	RESET	CTI	TIS	SLOCK

FIGURE 26

7	6	5	4	3	2	1	0
Reserved	Reserved	TXPWDN	TXBDEN	TXADEN	TXSYNC	RAPWDN	RBPWDN

FIGURE 27

7	6	5	4	3	2	1	0
Reserved	UP[2]	UP[1]	UP[0]	UDF	UA[2]	UA[1]	UA[0]

FIGURE 28

7	6	5	4	3	2	1	0
UAA	ETXRXA	RBLA	RBPA	RBRA	RALA	RAPA	RARA

FIGURE 29

7	6	5	4	3	2	1	0
UAAIE	ETXRXAIE	RBLAIE	RBPAIE	RBRAIE	RALAIE	RAPAIE	RARAIE

FIGURE 30

7	6	5	4	3	2	1	0
RDSLKOV	SCDIS	CEN	ECCA	ECCB	ABSC	LBA	FTXSCR

FIGURE 31

7	6	5	4	3	2	1	0
TXLL[7]	TXLL[6]	TXLL[5]	TXLL[4]	TXLL[3]	TXLL[2]	TXLL[1]	TXLL[0]

FIGURE 32

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	LLOSC	LLOSA	LLOSB	ETXBR

FIGURE 33

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	LLOSCIE	LLOSAIE	LLOSBIE	ETXBRIE

FIGURE 34

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ETXSD

FIGURE 35

	7	6	5	4	3	2	1	0
ETXD7 0x0D	ETXD7[7]	ETXD7[6]	ETXD7[5]	ETXD7[4]	ETXD7[3]	ETXD7[2]	ETXD7[1]	ETXD7[0]
ETXD6 0x0E	ETXD6[7]	ETXD6[6]	ETXD6[5]	ETXD6[4]	ETXD6[3]	ETXD6[2]	ETXD6[1]	ETXD6[0]
ETXD5 0x0F	ETXD5[7]	ETXD5[6]	ETXD5[5]	ETXD5[4]	ETXD5[3]	ETXD5[2]	ETXD5[1]	ETXD5[0]
ETXD4 0x10	ETXD4[7]	ETXD4[6]	ETXD4[5]	ETXD4[4]	ETXD4[3]	ETXD4[2]	ETXD4[1]	ETXD4[0]
ETXD3 0x11	ETXD3[7]	ETXD3[6]	ETXD3[5]	ETXD3[4]	ETXD3[3]	ETXD3[2]	ETXD3[1]	ETXD3[0]
ETXD2 0x12	ETXD2[7]	ETXD2[6]	ETXD2[5]	ETXD2[4]	ETXD2[3]	ETXD2[2]	ETXD2[1]	ETXD2[0]
ETXD1 0x13	ETXD1[7]	ETXD1[6]	ETXD1[5]	ETXD1[4]	ETXD1[3]	ETXD1[2]	ETXD1[1]	ETXD1[0]
ETXD0 0x14	ETXD0[7]	ETXD0[6]	ETXD0[5]	ETXD0[4]	ETXD0[3]	ETXD0[2]	ETXD0[1]	ETXD0[0]

FIGURE 36

7	6	5	4	3	2	1	0
DDR[3]	DDR[2]	DDR[1]	DDR[0]	IO[3]	IO[2]	IO[1]	IO[0]

FIGURE 37

7	6	5	4	3	2	1	0
EBRST[3]	EBRST[2]	EBRST[1]	EBRST[0]	ERFHEC	ERCHEC	ERBIP	TXPRBS

FIGURE 38

	7	6	5	4	3	2	1	0
EEEBIP1 0X17	EBIP1[7]	EBIP1[6]	EBIP1[5]	EBIP1[4]	EBIP1[3]	EBIP1[2]	EBIP1[1]	EBIP1[0]
ERRBIP0 0X18	EBIP0[7]	EBIP0[6]	EBIP0[5]	EBIP0[4]	EBIP0[3]	EBIP0[2]	EBIP0[1]	EBIP0[0]

FIGURE 39

7	6	5	4	3	2	1	0
EHEC[7]	EHEC[6]	EHEC[5]	EHEC[4]	EHEC[3]	EHEC[2]	EHEC[1]	EHEC[0]

FIGURE 40

7	6	5	4	3	2	1	0
Reserved	LNEN	LNSEL	LCLA	LCLB	TXLVLB	D2ULB	U2DLB

FIGURE 41

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	LBMP[4]	LBMP[3]	LBMP[2]	LBMP[1]	LBMP[0]

FIGURE 42

	7	6	5	4	3	2	1	0
ALBCF3 **0x1C**	ALBCF3[7]	ALBCF3[6]	ALBCF3[5]	ALBCF3[4]	ALBCF3[3]	ALBCF3[2]	ALBCF3[1]	ALBCF3[0]
ALBCF2 **0x1D**	ALBCF2[7]	ALBCF2[6]	ALBCF2[5]	ALBCF2[4]	ALBCF2[3]	ALBCF2[2]	ALBCF2[1]	ALBCF2[0]
ALBCF1 **0x1E**	ALBCF1[7]	ALBCF1[6]	ALBCF1[5]	ALBCF1[4]	ALBCF1[3]	ALBCF1[2]	ALBCF1[1]	ALBCF1[0]
ALBCF0 **0x1F**	ALBCF0[7]	ALBCF0[6]	ALBCF0[5]	ALBCF0[4]	ALBCF0[3]	ALBCF0[2]	ALBCF0[1]	ALBCF0[0]

FIGURE 43

7	6	5	4	3	2	1	0
RALL[7]	RALL[6]	RALL[5]	RALL[4]	RALL[3]	RALL[2]	RALL[1]	RALL[0]

FIGURE 44

7	6	5	4	3	2	1	0
RAELL[7]	RAELL[6]	RAELL[5]	RAELL[4]	RAELL[3]	RAELL[2]	RAELL[1]	RAELL[0]

FIGURE 45

7	6	5	4	3	2	1	0
Reserved	RALLC	RALLM	RALCS	RALDSLL	RALTCLL	RALFLL	ERABF

FIGURE 46

7	6	5	4	3	2	1	0
Reserved	RALLCIE	RALLMIE	RALCSIE	RALDSLLIE	RALTCLLIE	RALFLLIE	ERABFIE

FIGURE 47

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	RAESS	RABEC	RADFLK	RACDIS

FIGURE 48

	7	6	5	4	3	2	1	0
ERAD7 0x26	ERAD7[7]	ERAD7[6]	ERAD7[5]	ERAD7[4]	ERAD7[3]	ERAD7[2]	ERAD7[1]	ERAD7[0]
ERAD6 0x27	ERAD6[7]	ERAD6[6]	ERAD6[5]	ERAD6[4]	ERAD6[3]	ERAD6[2]	ERAD6[1]	ERAD6[0]
ERAD5 0x28	ERAD5[7]	ERAD5[6]	ERAD5[5]	ERAD5[4]	ERAD5[3]	ERAD5[2]	ERAD5[1]	ERAD5[0]
ERAD4 0x29	ERAD4[7]	ERAD4[6]	ERAD4[5]	ERAD4[4]	ERAD4[3]	ERAD4[2]	ERAD4[1]	ERAD4[0]
ERAD3 0x2A	ERAD3[7]	ERAD3[6]	ERAD3[5]	ERAD3[4]	ERAD3[3]	ERAD3[2]	ERAD3[1]	ERAD3[0]
ERAD2 0x2B	ERAD2[7]	ERAD2[6]	ERAD2[5]	ERAD2[4]	ERAD2[3]	ERAD2[2]	ERAD2[1]	ERAD2[0]
ERAD1 0x2C	ERAD1[7]	ERAD1[6]	ERAD1[5]	ERAD1[4]	ERAD1[3]	ERAD1[2]	ERAD1[1]	ERAD1[0]
ERAD0 0x2D	ERAD0[7]	ERAD0[6]	ERAD0[5]	ERAD0[4]	ERAD0[3]	ERAD0[2]	ERAD0[1]	ERAD0[0]

FIGURE 49

	7	6	5	4	3	2	1	0
RAHECC2 0x2E	RAHECC2[7]	RAHECC2[6]	RAHECC2[5]	RAHECC2[4]	RAHECC2[3]	RAHECC2[2]	RAHECC2[1]	RAHECC2[0]
RAHECC1 0x2F	RAHECC1[7]	RAHECC1[6]	RAHECC1[5]	RAHECC1[4]	RAHECC1[3]	RAHECC1[2]	RAHECC1[1]	RAHECC1[0]
RAHECC0 0x30	RAHECC0[7]	RAHECC0[6]	RAHECC0[5]	RAHECC0[4]	RAHECC0[3]	RAHECC0[2]	RAHECC0[1]	RAHECC0[0]

FIGURE 50

	7	6	5	4	3	2	1	0
RAHECT2 0x31	RAHECT2[7]	RAHECT2[6]	RAHECT2[5]	RAHECT2[4]	RAHECT2[3]	RAHECT2[2]	RAHECT2[1]	RAHECT2[0]
RAHECT1 0x32	RAHECT1[7]	RAHECT1[6]	RAHECT1[5]	RAHECT1[4]	RAHECT1[3]	RAHECT1[2]	RAHECT1[1]	RAHECT1[0]
RAHECT0 0x33	RAHECT0[7]	RAHECT0[6]	RAHECT0[5]	RAHECT0[4]	RAHECT0[3]	RAHECT0[2]	RAHECT0[1]	RAHECT0[0]

FIGURE 51

	7	6	5	4	3	2	1	0
RABIPC2 0x34	RABIPC2[7]	RABIPC2[6]	RABIPC2[5]	RABIPC2[4]	RABIPC2[3]	RABIPC2[2]	RABIPC2[1]	RABIPC2[0]
RABIPC1 0x35	RABIPC1[7]	RABIPC1[6]	RABIPC1[5]	RABIPC1[4]	RABIPC1[3]	RABIPC1[2]	RABIPC1[1]	RABIPC1[0]
RABIPC0 0x36	RABIPC0[7]	RABIPC0[6]	RABIPC0[5]	RABIPC0[4]	RABIPC0[3]	RABIPC0[2]	RABIPC0[1]	RABIPC0[0]

FIGURE 52

	7	6	5	4	3	2	1	0
RABIPT2 0x37	RABIPT2[7]	RABIPT2[6]	RABIPT2[5]	RABIPT2[4]	RABIPT2[3]	RABIPT2[2]	RABIPT2[1]	RABIPT2[0]
RABIPT1 0x38	RABIPT1[7]	RABIPT1[6]	RABIPT1[5]	RABIPT1[4]	RABIPT1[3]	RABIPT1[2]	RABIPT1[1]	RABIPT1[0]
RABIPT0 0x39	RABIPT0[7]	RABIPT0[6]	RABIPT0[5]	RABIPT0[4]	RABIPT0[3]	RABIPT0[2]	RABIPT0[1]	RABIPT0[0]

FIGURE 53

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RAXHEC	RAXBIP

FIGURE 54

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RAXHECIE	RAXBIPIE

FIGURE 55

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	RARCS	RARLOSA	RARLOSB	RARBA	RARDSLL

FIGURE 56

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	RARCSIE	RARLOSAIE	RARLOSBIE	RARBAIE	RARDSLLIE

FIGURE 57

7	6	5	4	3	2	1	0
RAU2DLBC[7]	RAU2DLBC[6]	RAU2DLBC[5]	RAU2DLBC[4]	RAU2DLBC[3]	RAU2DLBC[2]	RAU2DLBC[1]	RAU2DLBC[0]

FIGURE 58

7	6	5	4	3	2	1	0
ALPHA[3]	ALPHA[2]	ALPHA[1]	ALPHA[0]	DELTA[3]	DELTA[2]	DELTA[1]	DELTA[0]

FIGURE 59

7	6	5	4	3	2	1	0
MU[3]	MU[2]	MU[1]	MU[0]	SIGMA[3]	SIGMA[2]	SIGMA[1]	SIGMA[0]

FIGURE 60

7	6	5	4	3	2	1	0
PSI[3]	PSI[2]	PSI[1]	PSI[0]	RHO[3]	RHO[2]	RHO[1]	RHO[0]

FIGURE 61

	7	6	5	4	3	2	1	0
RABEC2 0x43	RABEC2[7]	RABEC2[6]	RABEC2[5]	RABEC2[4]	RABEC2[3]	RABEC2[2]	RABEC2[1]	RABEC2[0]
RABEC1 0x44	RABEC1[7]	RABEC1[6]	RABEC1[5]	RABEC1[4]	RABEC1[3]	RABEC1[2]	RABEC1[1]	RABEC1[0]
RABEC0 0x45	RABEC0[7]	RABEC0[6]	RABEC0[5]	RABEC0[4]	RABEC0[3]	RABEC0[2]	RABEC0[1]	RABEC0[0]

FIGURE 62

7	6	5	4	3	2	1	0
RBLL[7]	RBLL[6]	RBLL[5]	RBLL[4]	RBLL[3]	RBLL[2]	RBLL[1]	RBLL[0]

FIGURE 63

7	6	5	4	3	2	1	0
RBELL[7]	RBELL[6]	RBELL[5]	RBELL[4]	RBELL[3]	RBELL[2]	RBELL[1]	RBELL[0]

FIGURE 64

7	6	5	4	3	2	1	0
Reserved	RBLLC	RBLLM	RBLCS	RBLDSLL	RBLTCLL	RBLFLL	ERBBF

FIGURE 65

7	6	5	4	3	2	1	0
Reserved	RBLLCIE	RBLLMIE	RBLCSIE	RBLDSLLIE	RBLTCLLIE	RBLFLLIE	ERBBFIE

FIGURE 66

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	RBESS	RBBEC	RBDFLK	RBCDIS

FIGURE 67

	7	6	5	4	3	2	1	0
ERBD7 0x66	ERBD7[7]	ERBD7[6]	ERBD7[5]	ERBD7[4]	ERBD7[3]	ERBD7[2]	ERBD7[1]	ERBD7[0]
ERBD6 0x67	ERBD6[7]	ERBD6[6]	ERBD6[5]	ERBD6[4]	ERBD6[3]	ERBD6[2]	ERBD6[1]	ERBD6[0]
ERBD5 0x68	ERBD5[7]	ERBD5[6]	ERBD5[5]	ERBD5[4]	ERBD5[3]	ERBD5[2]	ERBD5[1]	ERBD5[0]
ERBD4 0x69	ERBD4[7]	ERBD4[6]	ERBD4[5]	ERBD4[4]	ERBD4[3]	ERBD4[2]	ERBD4[1]	ERBD4[0]
ERBD3 0x6A	ERBD3[7]	ERBD3[6]	ERBD3[5]	ERBD3[4]	ERBD3[3]	ERBD3[2]	ERBD3[1]	ERBD3[0]
ERBD2 0x6B	ERBD2[7]	ERBD2[6]	ERBD2[5]	ERBD2[4]	ERBD2[3]	ERBD2[2]	ERBD2[1]	ERBD2[0]
ERBD1 0x6C	ERBD1[7]	ERBD1[6]	ERBD1[5]	ERBD1[4]	ERBD1[3]	ERBD1[2]	ERBD1[1]	ERBD1[0]
ERBD0 0x6D	ERBD0[7]	ERBD0[6]	ERBD0[5]	ERBD0[4]	ERBD0[3]	ERBD0[2]	ERBD0[1]	ERBD0[0]

FIGURE 68

	7	6	5	4	3	2	1	0
RBHECC2 0x6E	RBHECC2[7]	RBHECC2[6]	RBHECC2[5]	RBHECC2[4]	RBHECC2[3]	RBHECC2[2]	RBHECC2[1]	RBHECC2[0]
RBHECC1 0x6F	RBHECC1[7]	RBHECC1[6]	RBHECC1[5]	RBHECC1[4]	RBHECC1[3]	RBHECC1[2]	RBHECC1[1]	RBHECC1[0]
RBHECC0 0x70	RBHECC0[7]	RBHECC0[6]	RBHECC0[5]	RBHECC0[4]	RBHECC0[3]	RBHECC0[2]	RBHECC0[1]	RBHECC0[0]

FIGURE 69

	7	6	5	4	3	2	1	0
RBHECT2 0x71	RBHECT2[7]	RBHECT2[6]	RBHECT2[5]	RBHECT2[4]	RBHECT2[3]	RBHECT2[2]	RBHECT2[1]	RBHECT2[0]
RBHECT1 0x72	RBHECT1[7]	RBHECT1[6]	RBHECT1[5]	RBHECT1[4]	RBHECT1[3]	RBHECT1[2]	RBHECT1[1]	RBHECT1[0]
RBHECT0 0x73	RBHECT0[7]	RBHECT0[6]	RBHECT0[5]	RBHECT0[4]	RBHECT0[3]	RBHECT0[2]	RBHECT0[1]	RBHECT0[0]

FIGURE 70

	7	6	5	4	3	2	1	0
RBBIPC2 0x74	RBBIPC2[7]	RBBIPC2[6]	RBBIPC2[5]	RBBIPC2[4]	RBBIPC2[3]	RBBIPC2[2]	RBBIPC2[1]	RBBIPC2[0]
RBBIPC1 0x75	RBBIPC1[7]	RBBIPC1[6]	RBBIPC1[5]	RBBIPC1[4]	RBBIPC1[3]	RBBIPC1[2]	RBBIPC1[1]	RBBIPC1[0]
RBBIPC0 0x76	RBBIPC0[7]	RBBIPC0[6]	RBBIPC0[5]	RBBIPC0[4]	RBBIPC0[3]	RBBIPC0[2]	RBBIPC0[1]	RBBIPC0[0]

FIGURE 71

	7	6	5	4	3	2	1	0
RBBIPT2 0x77	RBBIPT2[7]	RBBIPT2[6]	RBBIPT2[5]	RBBIPT2[4]	RBBIPT2[3]	RBBIPT2[2]	RBBIPT2[1]	RBBIPT2[0]
RBBIPT1 0x78	RBBIPT1[7]	RBBIPT1[6]	RBBIPT1[5]	RBBIPT1[4]	RBBIPT1[3]	RBBIPT1[2]	RBBIPT1[1]	RBBIPT1[0]
RBBIPT0 0x79	RBBIPT0[7]	RBBIPT0[6]	RBBIPT0[5]	RBBIPT0[4]	RBBIPT0[3]	RBBIPT0[2]	RBBIPT0[1]	RBBIPT0[0]

FIGURE 72

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RBXHEC	RBXBIP

FIGURE 73

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RBXHECIE	RBXBIPIE

FIGURE 74

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	RBRCS	RBRLOSA	RBRLOSB	RBRBA	RBRDSLL

FIGURE 75

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	RBRCSIE	RBRLOSAIE	RBRLOSBIE	RBRBAIE	RBRDSLLIE

FIGURE 76

7	6	5	4	3	2	1	0
RBU2DLBC[7]	RBU2DLBC[6]	RBU2DLBC[5]	RBU2DLBC[4]	RBU2DLBC[3]	RBU2DLBC[2]	RBU2DLBC[1]	RBU2DLBC[0]

FIGURE 77

7	6	5	4	3	2	1	0
ALPHA[3]	ALPHA[2]	ALPHA[1]	ALPHA[0]	DELTA[3]	DELTA[2]	DELTA[1]	DELTA[0]

FIGURE 78

7	6	5	4	3	2	1	0
MU[3]	MU[2]	MU[1]	MU[0]	SIGMA[3]	SIGMA[2]	SIGMA[1]	SIGMA[0]

FIGURE 79

7	6	5	4	3	2	1	0
PSI[3]	PSI[2]	PSI[1]	PSI[0]	RHO[3]	RHO[2]	RHO[1]	RHO[0]

FIGURE 80

	7	6	5	4	3	2	1	0
RBBEC2 0x83	RBBEC2[7]	RBBEC2[6]	RBBEC2[5]	RBBEC2[4]	RBBEC2[3]	RBBEC2[2]	RBBEC2[1]	RBBEC2[0]
RBBEC1 0x84	RBBEC1[7]	RBBEC1[6]	RBBEC1[5]	RBBEC1[4]	RBBEC1[3]	RBBEC1[2]	RBBEC1[1]	RBBEC1[0]
RBBEC0 0x85	RBBEC0[7]	RBBEC0[6]	RBBEC0[5]	RBBEC0[4]	RBBEC0[3]	RBBEC0[2]	RBBEC0[1]	RBBEC0[0]

FIGURE 81

7	6	5	4	3	2	1	0
Reserved	Reserved	CLVM[1]	CLVM[0]	BWIDTH	Reserved	UBDEN	UMODE

FIGURE 82

	7	6	5	4	3	2	1	0
UCPL3 0xA1	Reserved	UCPL3[6]	UCPL3[5]	UCPL3[4]	UCPL3[3]	UCPL3[2]	UCPL3[1]	UCPL3[0]
UCPL2 0xA2	UCPL2[7]	UCPL2[6]	UCPL2[5]	UCPL2[4]	UCPL2[3]	UCPL2[2]	UCPL2[1]	UCPL2[0]
UCPL1 0xA3	UCPL1[7]	UCPL1[6]	UCPL1[5]	UCPL1[4]	UCPL1[3]	UCPL1[2]	UCPL1[1]	UCPL1[0]
UCPL0 0xA4	UCPL0[7]	UCPL0[6]	UCPL0[5]	UCPL0[4]	UCPL0[3]	UCPL0[2]	UCPL0[1]	UCPL0[0]

FIGURE 83

7	6	5	4	3	2	1	0
UCSPL[7]	UCSPL[6]	UCSPL[5]	UCSPL[4]	UCSPL[3]	UCSPL[2]	UCSPL[1]	UCSPL[0]

FIGURE 84

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	USPAL[4]	USPAL[3]	USPAL[2]	USPAL[1]	USPAL[0]

FIGURE 85

7	6	5	4	3	2	1	0
USPAM[7]	USPAM[6]	USPAM[5]	USPAM[4]	USPAM[3]	USPAM[2]	USPAM[1]	USPAM[0]

FIGURE 86

	7	6	5	4	3	2	1	0
MTBQT30 0xA9	MTBQT30[7]	MTBQT30[6]	MTBQT30[5]	MTBQT30[4]	MTBQT30[3]	MTBQT30[2]	MTBQT30[1]	MTBQT30[0]
MTBQT29 0xAA	MTBQT29[7]	MTBQT29[6]	MTBQT29[5]	MTBQT29[4]	MTBQT29[3]	MTBQT29[2]	MTBQT29[1]	MTBQT29[0]
MTBQT2 0xC5	MTBQT2[7]	MTBQT2[6]	MTBQT2[5]	MTBQT2[4]	MTBQT2[3]	MTBQT2[2]	MTBQT2[1]	MTBQT2[0]
MTBQT1 0xC6	MTBQT1[7]	MTBQT1[6]	MTBQT1[5]	MTBQT1[4]	MTBQT1[3]	MTBQT1[2]	MTBQT1[1]	MTBQT1[0]
MTBQT0 0xC7	MTBQT0[7]	MTBQT0[6]	MTBQT0[5]	MTBQT0[4]	MTBQT037]	MTBQT0[2]	MTBQT0[1]	MTBQT0[0]

FIGURE 87

	7	6	5	4	3	2	1	0
MTBQFL3 0xC8	MTBQFL3[7]	MTBQFL3[6]	MTBQFL3[5]	MTBQFL3[4]	MTBQFL3[3]	MTBQFL3[2]	MTBQFL3[1]	MTBQFL3[0]
MTBQFL2 0xC9	MTBQFL2[7]	MTBQFL2[6]	MTBQFL2[5]	MTBQFL2[4]	MTBQFL2[3]	MTBQFL2[2]	MTBQFL2[1]	MTBQFL2[0]
MTBQFL1 0xCA	MTBQFL1[7]	MTBQFL1[6]	MTBQFL1[5]	MTBQFL1[4]	MTBQFL1[3]	MTBQFL1[2]	MTBQFL1[1]	MTBQFL1[0]
MTBQFL0 0xCB	MTBQFL0[7]	MTBQFL0[6]	MTBQFL0[5]	MTBQFL0[4]	MTBQFL0[3]	MTBQFL0[2]	MTBQFL0[1]	MTBQFL0[0]

FIGURE 88

	7	6	5	4	3	2	1	0
MTBQE3 0xCC	Reserved	MTBQE3[6]	MTBQE3[5]	MTBQE3[4]	MTBQE3[3]	MTBQE3[2]	MTBQE3[1]	MTBQE3[0]
MTBQE2 0xCD	MTBQE2[7]	MTBQE2[6]	MTBQE2[5]	MTBQE2[4]	MTBQE2[3]	MTBQE2[2]	MTBQE2[1]	MTBQE2[0]
MTBQE1 0xCE	MTBQE1[7]	MTBQE1[6]	MTBQE1[5]	MTBQE1[4]	MTBQE1[3]	MTBQE1[2]	MTBQE1[1]	MTBQE1[0]
MTBQE0 0xCF	MTBQE0[7]	MTBQE0[6]	MTBQE0[5]	MTBQE0[4]	MTBQE0[3]	MTBQE0[2]	MTBQE0[1]	MTBQE0[0]

FIGURE 89

	7	6	5	4	3	2	1	0
MTBQF3 0D0	Reserved	MTBQF3[6]	MTBQF3[5]	MTBQF3[4]	MTBQF3[3]	MTBQF3[2]	MTBQF3[1]	MTBQF3[0]
MTBQF2 0xD1	MTBQF2[7]	MTBQF2[6]	MTBQF2[5]	MTBQF2[4]	MTBQF2[3]	MTBQF2[2]	MTBQF2[1]	MTBQF2[0]
MTBQF1 0xD2	MTBQF1[7]	MTBQF1[6]	MTBQF1[5]	MTBQF1[4]	MTBQF1[3]	MTBQF1[2]	MTBQF1[1]	MTBQF1[0]
MTBQF0 0xD3	MTBQF0[7]	MTBQF0[6]	MTBQF0[5]	MTBQF0[4]	MTBQF0[3]	MTBQF0[2]	MTBQF0[1]	MTBQF0[0]

FIGURE 90

	7	6	5	4	3	2	1	0
MTBCF3 0xD4	Reserved	MTBCF3[6]	MTBCF3[5]	MTBCF3[4]	MTBCF3[3]	MTBCF3[2]	MTBCF3[1]	MTBCF3[0]
MTBCF2 0xD5	MTBCF2[7]	MTBCF2[6]	MTBCF2[5]	MTBCF2[4]	MTBCF2[3]	MTBCF2[2]	MTBCF2[1]	MTBCF2[0]
MTBCF1 0xD6	MTBCF1[7]	MTBCF1[6]	MTBCF1[5]	MTBCF1[4]	MTBCF1[3]	MTBCF1[2]	MTBCF1[1]	MTBCF1[0]
MTBCF0 0xD7	MTBCF0[7]	MTBCF0[6]	MTBCF0[5]	MTBCF0[4]	MTBCF0[3]	MTBCF0[2]	MTBCF0[1]	MTBCF0[0]

FIGURE 91

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FIBFL	MTBFL

FIGURE 92

	7	6	5	4	3	2	1	0
MTBQOV3 0xD9	Reserved	MTBQOV3[6]	MTBQOV3[5]	MTBQOV3[4]	MTBQOV3[3]	MTBQOV3[2]	MTBQOV3[1]	MTBQOV3[0]
MTBQOV2 0xDA	MTBQOV2[7]	MTBQOV2[6]	MTBQOV2[5]	MTBQOV2[4]	MTBQOV2[3]	MTBQOV2[2]	MTBQOV2[1]	MTBQOV2[0]
MTBQOV1 0xDB	MTBQOV1[7]	MTBQOV1[6]	MTBQOV1[5]	MTBQOV1[4]	MTBQOV1[3]	MTBQOV1[2]	MTBQOV1[1]	MTBQOV1[0]
MTBQOV0 0xDC	MTBQOV0[7]	MTBQOV0[6]	MTBQOV0[5]	MTBQOV0[4]	MTBQOV0[3]	MTBQOV0[2]	MTBQOV0[1]	MTBQOV0[0]

FIGURE 93

7	6	5	4	3	2	1	0
D2ULBCC[7]	D2ULBCC[6]	D2ULBCC[5]	D2ULBCC[4]	D2ULBCC[3]	D2ULBCC[2]	D2ULBCC[1]	D2ULBCC[0]

FIGURE 94

7	6	5	4	3	2	1	0
PDULA	CTFRA	D2ULBC	U2DLBC	UPRTY	FIBOVA	MTBSOVA	MTBHOVA

FIGURE 95

7	6	5	4	3	2	1	0
PDULIE	CTFRIE	D2ULBCIE	U2DLBCIE	UPRTYIE	FIBOVAIE	MTBSOVAIE	MTBHOVAIE

FIGURE 96

	7	6	5	4	3	2	1	0
ALFLT3 0xF7	ALFLT3[7]	ALFLT3[6]	ALFLT3[5]	ALFLT3[4]	ALFLT3[3]	ALFLT3[2]	ALFLT3[1]	ALFLT3[0]
ALFLT2 0xF8	ALFLT2[7]	ALFLT2[6]	ALFLT2[5]	ALFLT2[4]	ALFLT2[3]	ALFLT2[2]	ALFLT2[1]	ALFLT2[0]
ALFLT1 0xF9	ALFLT1[7]	ALFLT1[6]	ALFLT1[5]	ALFLT1[4]	ALFLT1[3]	ALFLT1[2]	ALFLT1[1]	ALFLT1[0]
ALFLT0 0xFA	ALFLT0[7]	ALFLT0[6]	ALFLT0[5]	ALFLT0[4]	ALFLT0[3]	ALFLT0[2]	ALFLT0[1]	ALFLT0[0]

FIGURE 97

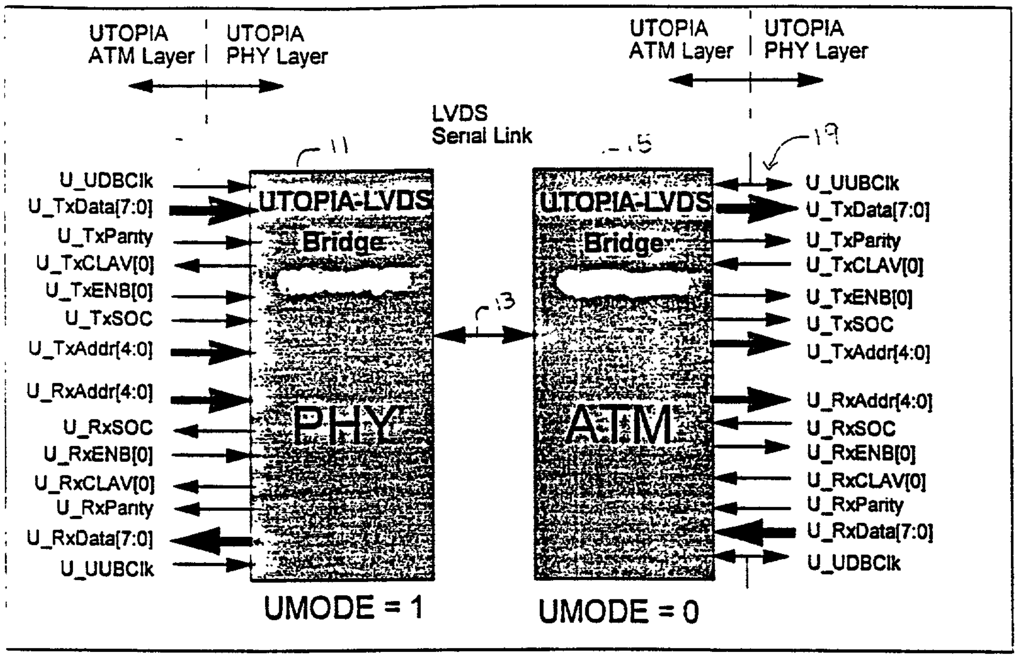


FIGURE 98

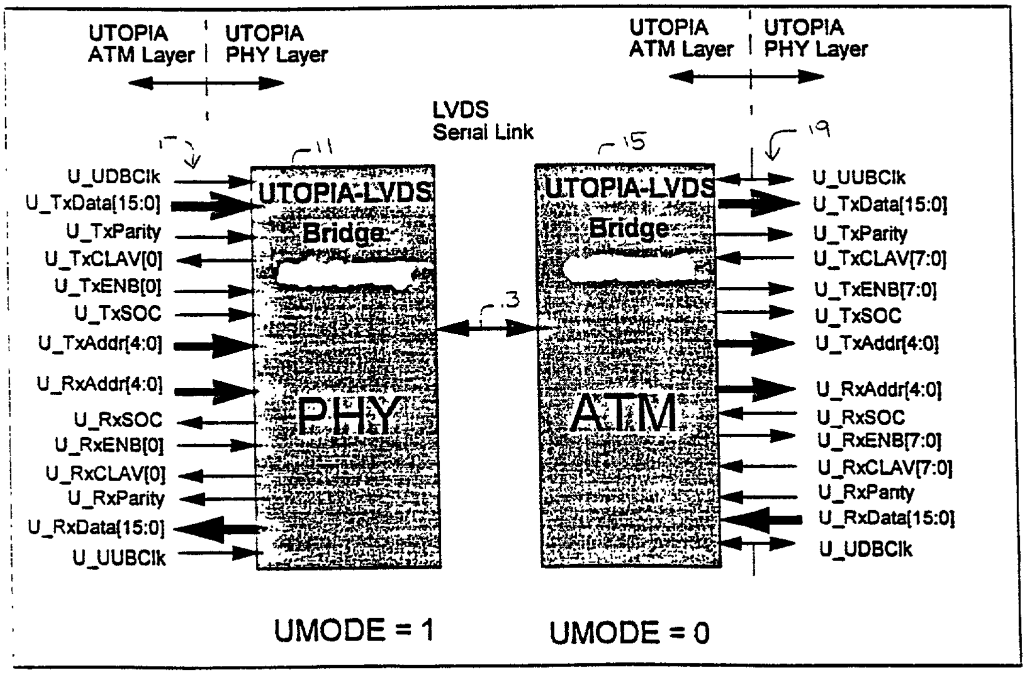


FIGURE 99

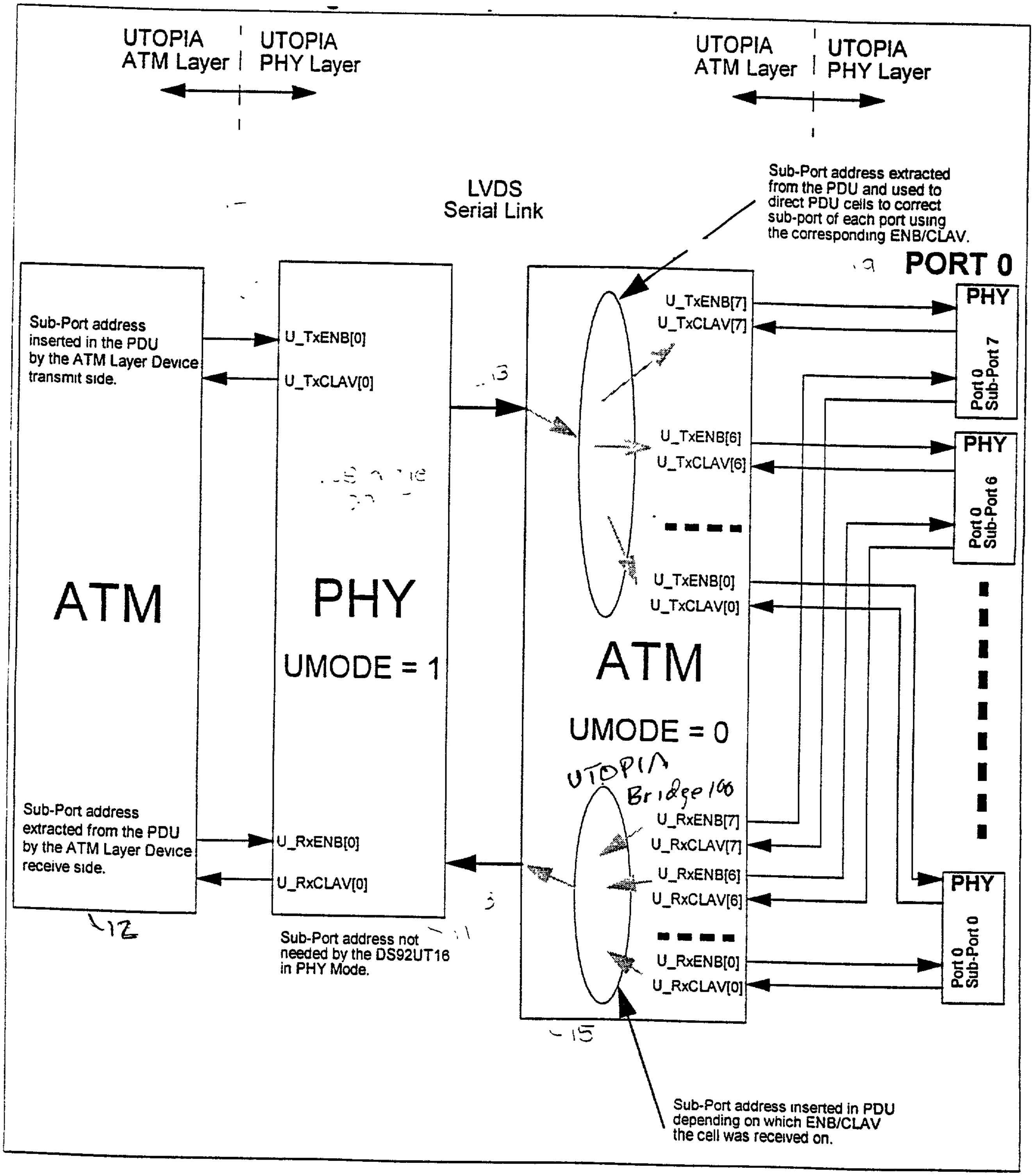

UTOPIA ATM Layer
UTOPIA PHY Layer
UTOPIA ATM Layer
UTOPIA PHY Layer
LVDS Serial Link
Sub-Port address extracted from the PDU and used to direct PDU cells to correct sub-port of each port using the corresponding ENB/CLAV.
PORT 0
Sub-Port address inserted in the PDU by the ATM Layer Device transmit side.
U_TxENB[0]
U_TxCLAV[0]
13
U_TxENB[7]
U_TxCLAV[7]
PHY
Port 0 Sub-Port 7
U_TxENB[6]
U_TxCLAV[6]
PHY
Port 0 Sub-Port 6
U_TxENB[0]
U_TxCLAV[0]
ATM
PHY
UMODE = 1
ATM
UMODE = 0
UTOPIA Bridge 100
Sub-Port address extracted from the PDU by the ATM Layer Device receive side.
U_RxENB[0]
U_RxCLAV[0]
U_RxENB[7]
U_RxCLAV[7]
U_RxENB[6]
U_RxCLAV[6]
U_RxENB[0]
U_RxCLAV[0]
PHY
Port 0 Sub-Port 0
12
Sub-Port address not needed by the DS92UT16 in PHY Mode.
15
Sub-Port address inserted in PDU depending on which ENB/CLAV the cell was received on.

FIGURE 100

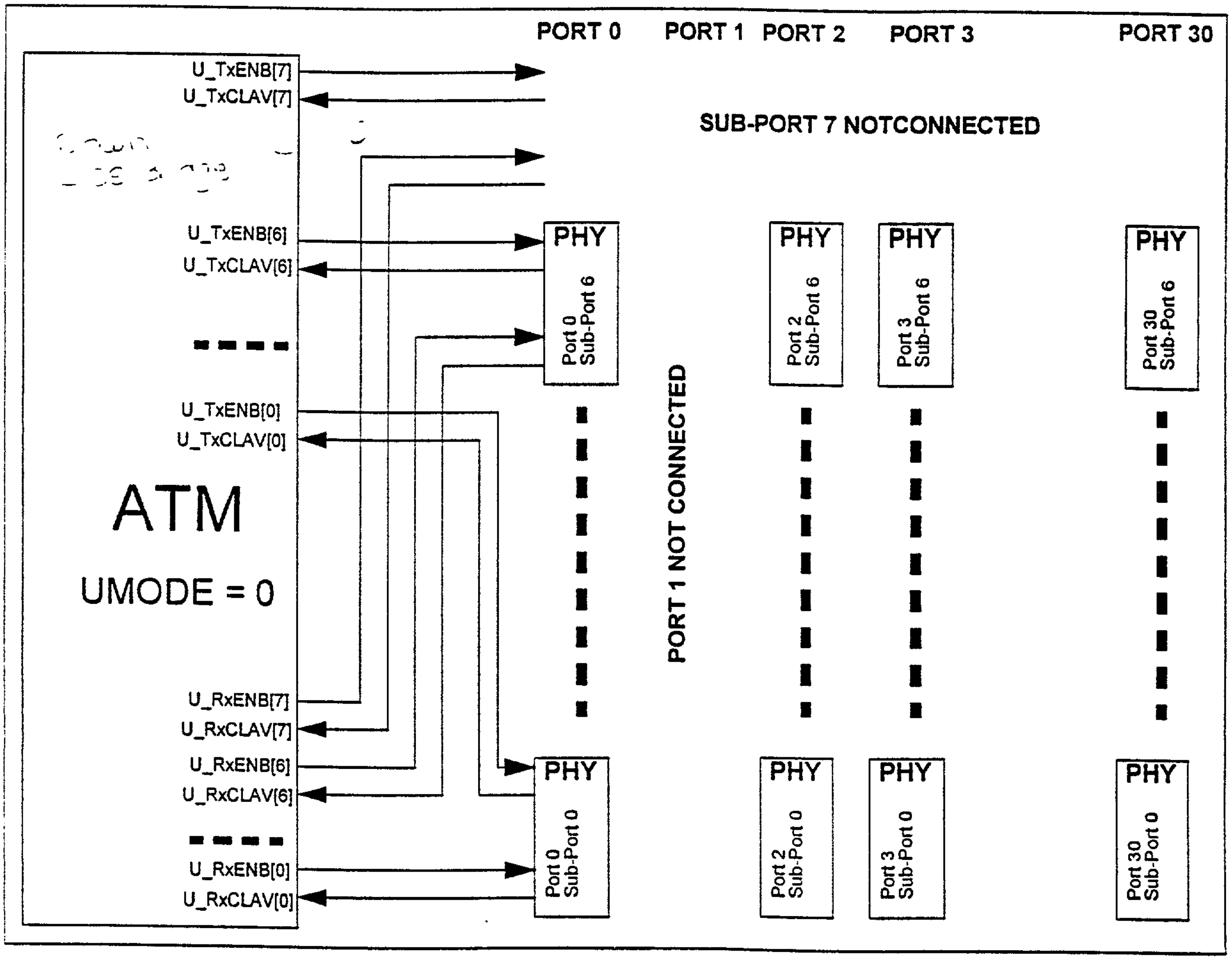

PORT 0
PORT 1
PORT 2
PORT 3
PORT 30
U_TxENB[7]
U_TxCLAV[7]
SUB-PORT 7 NOTCONNECTED
U_TxENB[6]
U_TxCLAV[6]
U_TxENB[0]
U_TxCLAV[0]
ATM
UMODE = 0
U_RxENB[7]
U_RxCLAV[7]
U_RxENB[6]
U_RxCLAV[6]
U_RxENB[0]
U_RxCLAV[0]
PHY
Port 0 Sub-Port 6
PHY
Port 2 Sub-Port 6
PHY
Port 3 Sub-Port 6
PHY
Port 30 Sub-Port 6
PORT 1 NOT CONNECTED
PHY
Port 0 Sub-Port 0
PHY
Port 2 Sub-Port 0
PHY
Port 3 Sub-Port 0
PHY
Port 30 Sub-Port 0

FIGURE 101

Number of Queues in use	Recommended Threshold
31	4
30	4
29	5
28	5
27	5
26	6
25	6
24	7
23	7
22	8
21	9
20	10
19	10
18	11
17	12
16	14
15	15
14	16
13	18
12	20
11	23
10	26
9	29
8	34
7	39
6	47
5	58
4	74
3	100
2	100
1	154

FIGURE 102

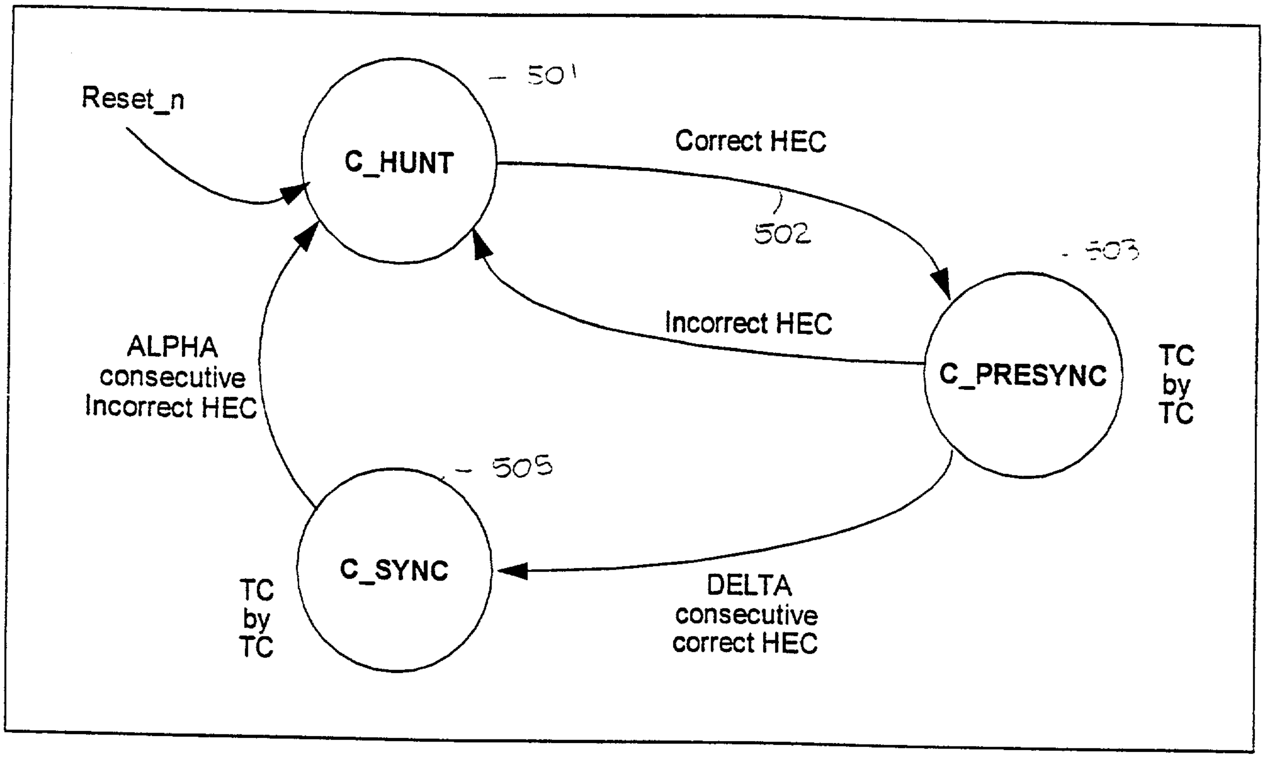


FIGURE 103

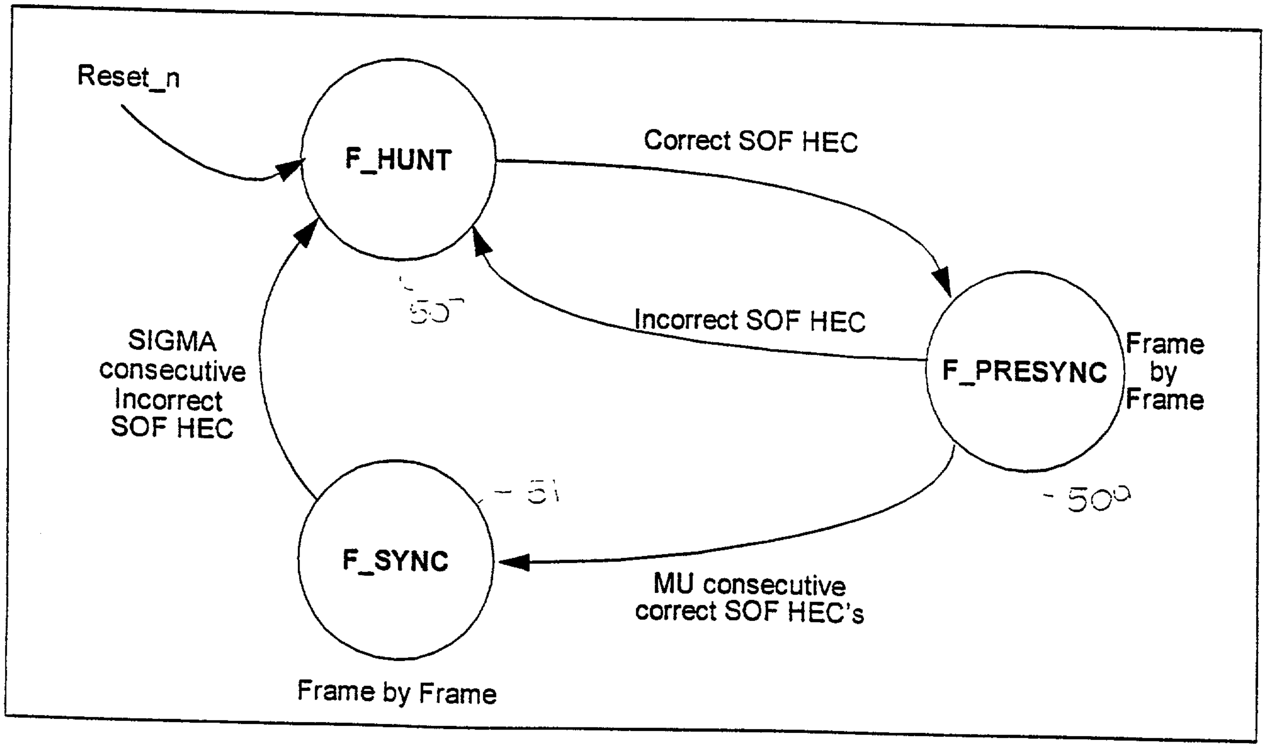


FIGURE 104

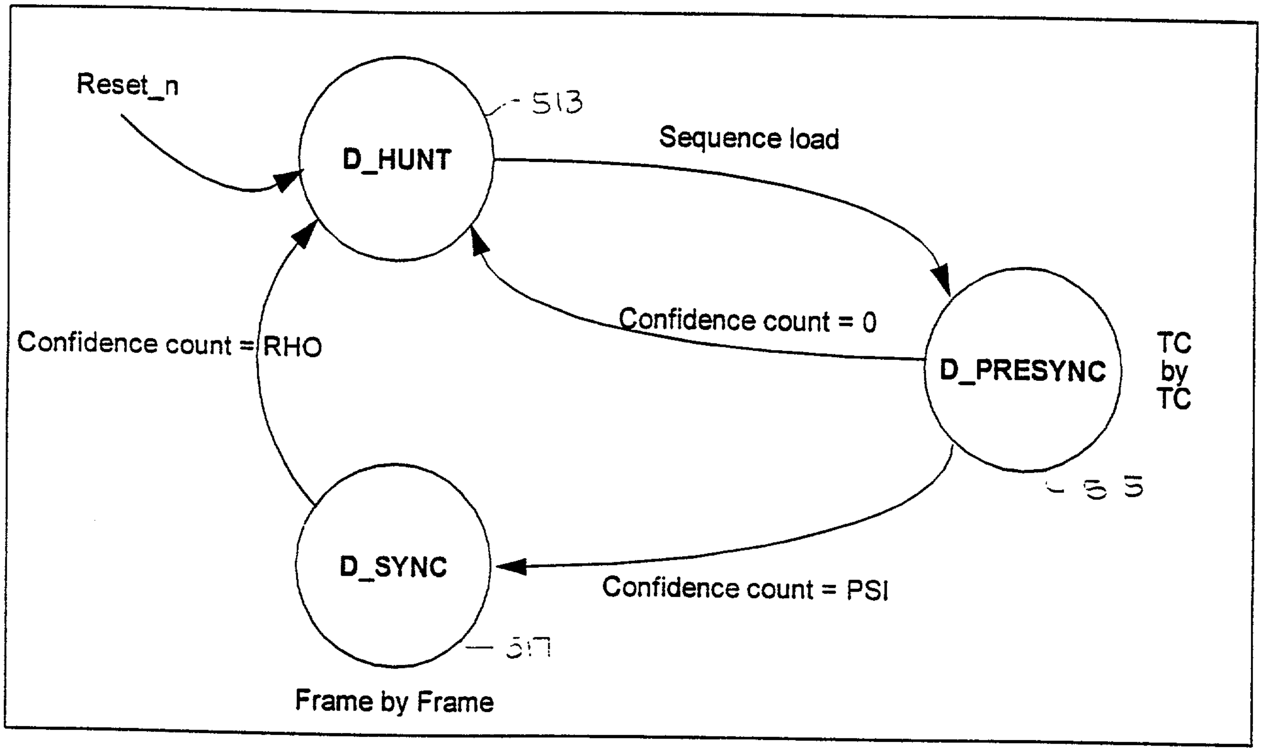

Reset_n
D_HUNT
513
Sequence load
Confidence count = 0
D_PRESYNC
TC
by
TC
515
Confidence count = RHO
D_SYNC
517
Confidence count = PSI
Frame by Frame

FIGURE 105

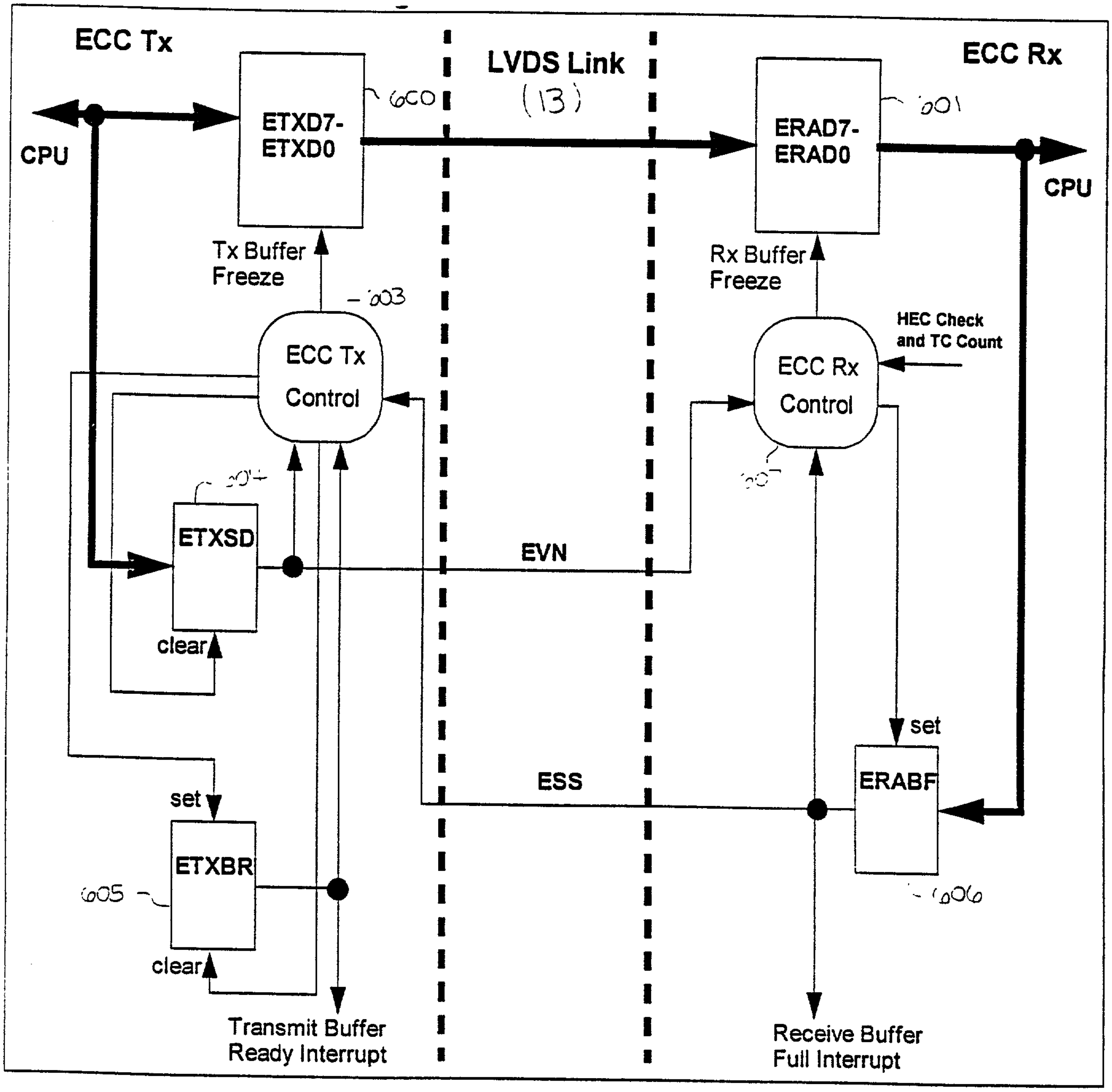

ECC Tx
LVDS Link
(13)
ECC Rx
CPU
ETXD7-
ETXD0
600
ERAD7-
ERAD0
601
CPU
Tx Buffer
Freeze
603
Rx Buffer
Freeze
HEC Check
and TC Count
ECC Tx
Control
ECC Rx
Control
602
604
ETXSD
EVN
clear
set
ERABF
ESS
set
ETXBR
605
606
clear
Transmit Buffer
Ready Interrupt
Receive Buffer
Full Interrupt

FIGURE 106

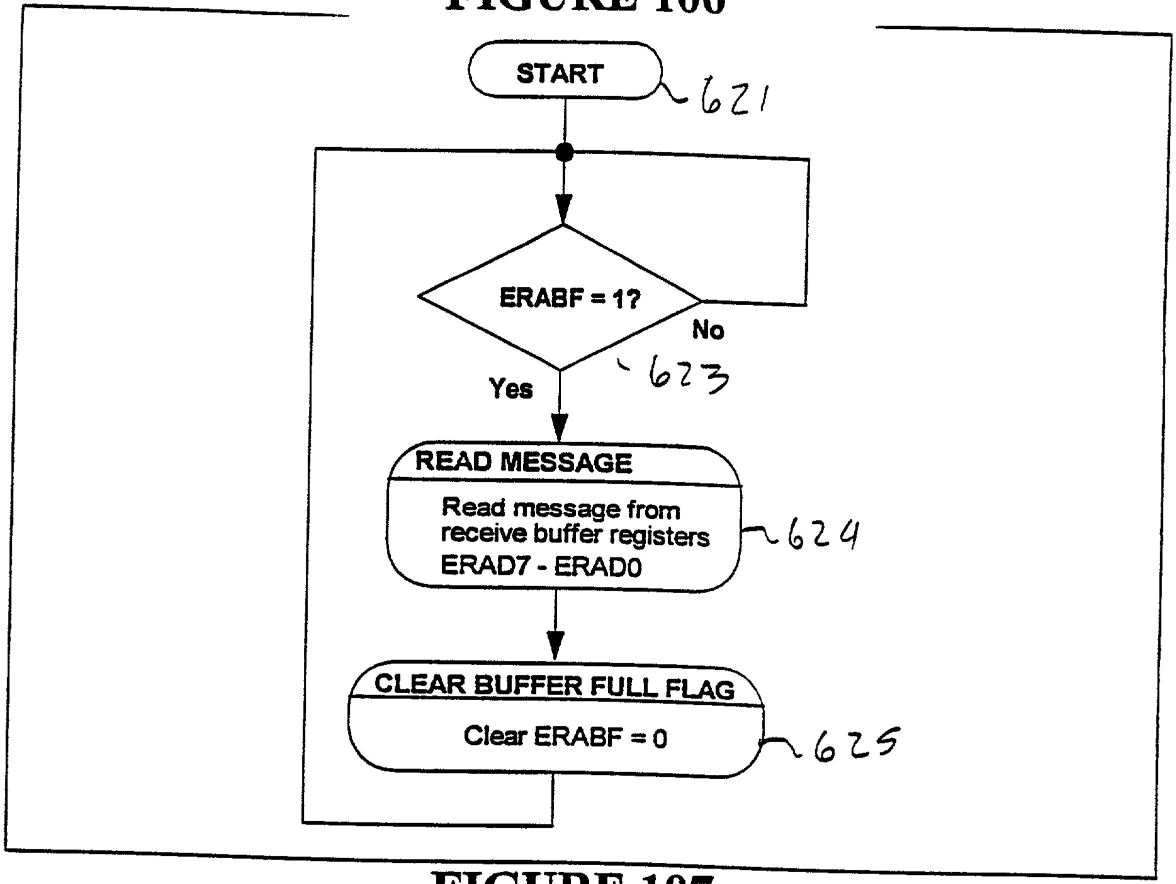


FIGURE 107

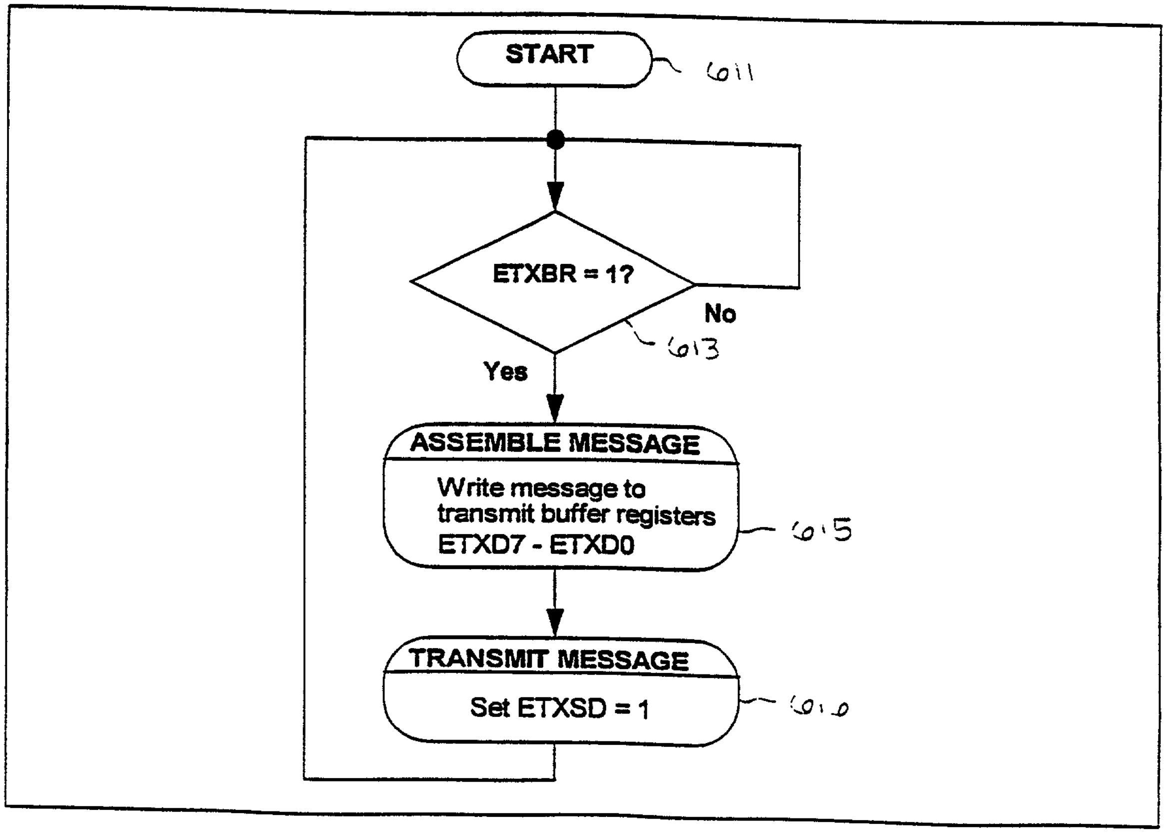
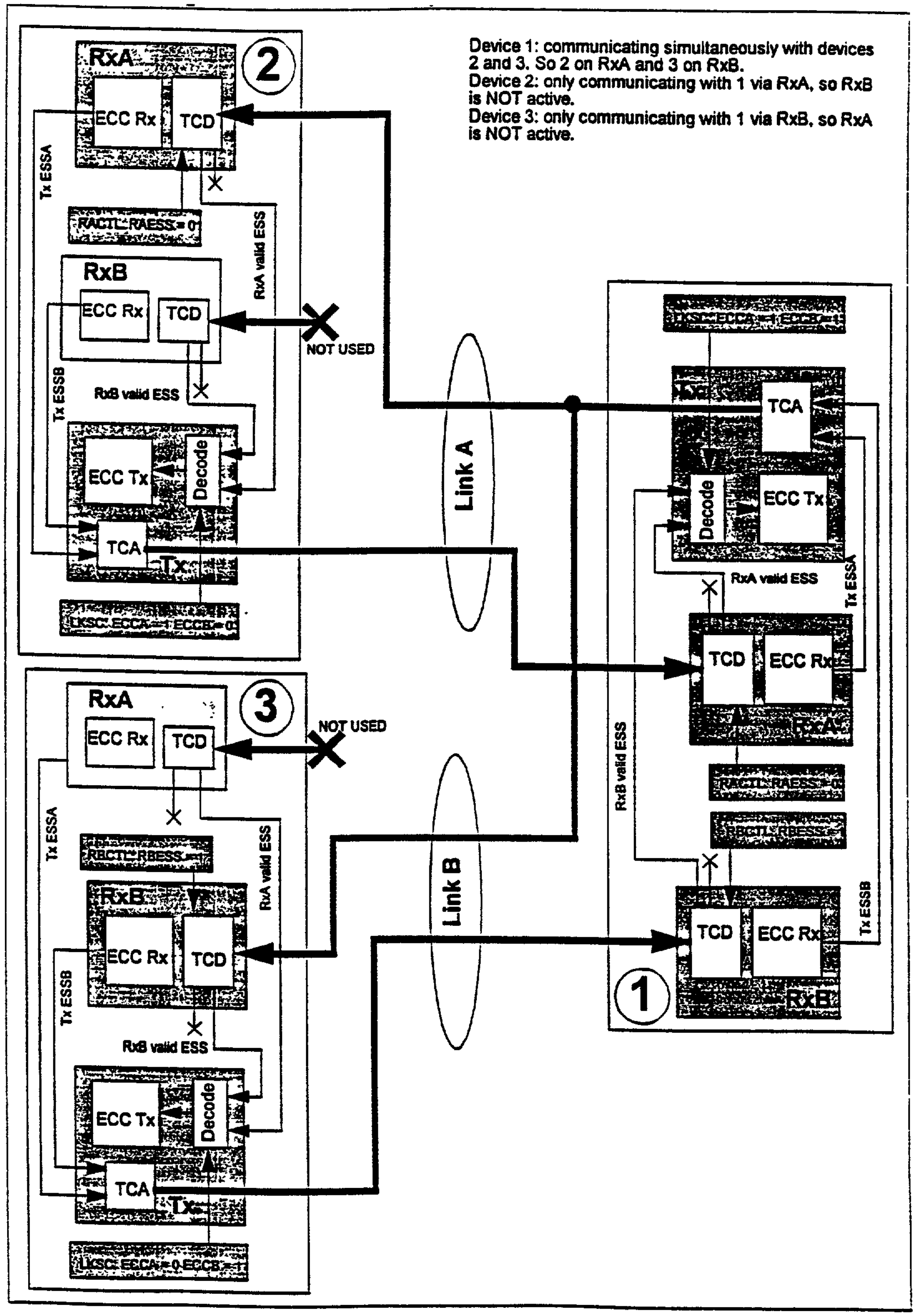


FIGURE 108



Device 1: communicating simultaneously with devices 2 and 3. So 2 on RxA and 3 on RxB.
Device 2: only communicating with 1 via RxA, so RxB is NOT active.
Device 3: only communicating with 1 via RxB, so RxA is NOT active.